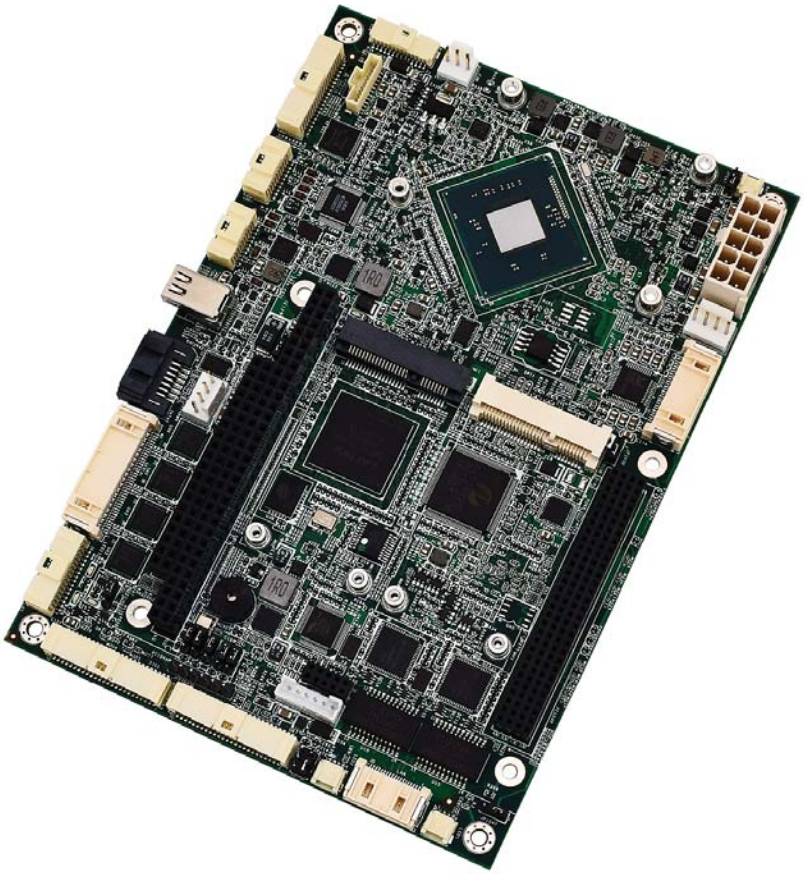
WinSystems®

The Embedded Systems Authority

EPX-C414

Intel® Atom™ EPIC Single Board Computer

Product Manual



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Revision History

Document Version	Last Updated Date	Brief Description of Change
v1.0	9/2017	Initial release
v1.1	9/2017	Correct JPSATA table and LVDS connector part number
v1.2	7/29/2025	Updated Conformal Coating, added Warranty link, updated all links

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Trademark Acknowledgments

Table of Contents

1. Before You Begin

Review the warnings in this section and the best practice recommendations (see “Best Practices” on page 66) when using and handling the WinSystems EPX-C414. Following these recommendations provides an optimal user experience and prevents damage. Read through this document and become familiar with the EPX-C414 before proceeding.

APPLYING CONFORMAL COATING AFTER PURCHASE WILL VOID YOUR WARRANTY. FAILING TO COMPLY WITH THESE BEST PRACTICES MAY DAMAGE THE PRODUCT AND VOID YOUR WARRANTY.

1.1 Warnings

Only qualified personnel should configure and install the EPX-C414. While observing the best practices, pay particular attention to the following waning.

Avoid Electrostatic Discharge (ESD)
Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

2. Introduction

This manual provides configuration and usage information for the EPX-C414. If you still have questions, contact Technical Support at (817) 274-7553, Monday through Friday, between 8 AM and 5 PM Central Standard Time (CST).

Refer to the WinSystems website for other accessories (including cable drawings and pinouts) that can be used with your EPX-C414.

3. Functionality

The EPX-C414 is an Intel® ATOM™ Single Board Computer (SBC) which uses either a 1.33 GHz dual-core Intel E3825 or a 1.91 GHz quad-core Intel E3845 processor. This EPIC-compatible unit incorporates a pair of 10/100/1000 Mbps Ethernet controllers, 1 SATA channel, 48 lines of digital I/O, 4 serial RS- 232/422/485 ports, a watchdog timer, and LPT. The SBC also supports HD audio and 8 USB ports, and is equipped with a CFast socket and 2 MiniPCIe card sockets.

The EPX-C414 board supports up to 8 GB DDR3L SODIMM system memory via an on-board socket located at CDIMM.

NOTE WinSystems can provide custom configurations for OEM clients. Please contact an Application Engineer for details.

4. Features

The EPX-C414 provides the following features.

Single Board Computer

- Multi-Core Intel® Atom™ E3800 processors
  - E3825 2 core, 1.33 GHz
  - E3845 4 core, 1.91 GHz

Operating Systems (compatibility)

- Windows Embedded Standard 7,8
- Windows 10 and 10 IoT Enterprise (32/64-bit)
- Linux
- DOS
- Other x86-compatible

Memory

- Up to 8 GB DDR3L SODIMM (socketed)
  - 1066 MHz (E3826)
  - 1333 MHz (E3845)

BIOS

- InsydeH2O® UEFI BIOS

Video Interfaces (supports dual simultaneous displays)

- Up to 24 bpp color panel support
- Analog VGA resolution up to 2560 x 1600 at 60 Hz
- Flat-panel resolution up to 1920 x 1200 in dual bus mode
- Low-voltage differential signaling (LVDS)
- Mini DisplayPort (version 1.1)
  - 2560 x 1440 at 60 Hz
  - 4k at 30 Hz

Ethernet

- 2 Intel® 10/100/1000 Mbps controllers using Intel i210

Storage

- 1 SATA (2.0) channel
- 1 MB soldered-on SRAM with battery back-up

- mSATA SSD optionally supported at MiniPCIe socket
- CFast SSD socket

Digital Input/Output

- 48 GPIO bidirectional lines

Bus Expansion

- PC/104
- PC/104-*Plus*
- 2x MiniPCIe (1 socket supports mSATA SSD)

Serial Interface

- 4 serial ports (RS-232/422/485)

Line Printer Port

- SPP/EPP supported

USB

- 8 USB 2.0 ports

Audio

- Hi-definition (HD) audio supported

Power

- +5V DC required

Industrial Operating Temperature

- -40 to +85°C

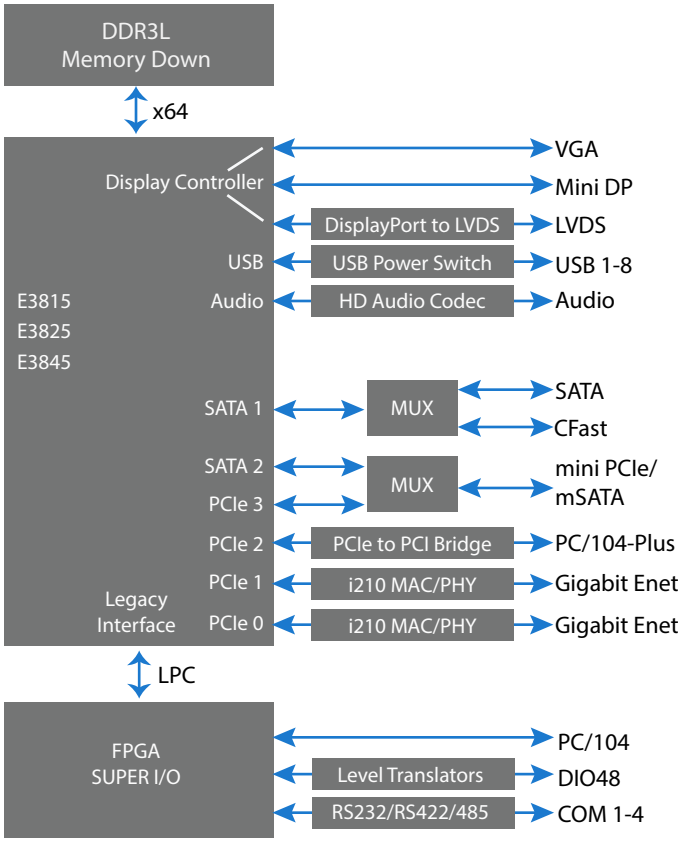
Additional Features

- Watchdog timer adjustable from 1 second to 255 minute reset
- RoHS compliant
- Backlight power supported
- Custom splash screen on start-up
- Real-time clock/calendar

5. General Operation

5.1 System Block Diagram

The EPX-C414 is a single-board computer (SBC). It is a full-featured embedded system with a variety of on-board I/O options. The following figure is a simplified system block diagram of the EPX-C414.



Three display interfaces (mini DisplayPort, VGA, and LVDS) support up to two independent displays, along with stereo audio. Communication interfaces include two Gigabit Ethernet (Intel i210) ports, eight USB 2.0 ports, and four serial RS-232/422/485 channels. 48 digital I/O lines are individually programmable for input, output, or interrupt-driven applications. The first 24 lines are capable of fully latched event sensing with software-programmable polarity. For additional flexibility, the I/O lines can be paired with external isolation and relay modules.

The EPX-C414 provides an upgrade for existing PC/104-Plus compatible single board computers. Its designed for harsh environments and reliability, with an optional solution for operating temperatures between -40 and +85°C (-40 and +185°F).

The EPX-C414 processor options provide single, dual, or quad-core processing. Each processor option is available with up to 8 GB of socketed DDR3L memory and non-stack-through PC/104-Plus connectors. 1 MB of external battery-backed SRAM is available at an interface provided by the FPGA.

Two full-sized miniPCIe sockets support USB, with one wired to support mSATA. Linux, Windows, and other x86 operating systems can be initialized from the SATA, mSATA, or USB interfaces. This provides flexible data storage options.

6. Specifications

The EPX-C414 adheres to the following specifications and requirements.

Table 1: EPX-C414 Specifications

Model	EPX-C414-3825-0	EPX-C414-3845-0
Electrical Specifications		
Model description	EPIC SBC E3825 SOC with heat sink	EPIC SBC E3845 SOC with heat sink
Processor	E3825 dual core 1.33 GHz, 1 MB cache	E3845 quad core 1.91 GHz, 2 MB cache
Power	+5V DC +/- 5% Max: 1.9A Typical: 1.5A S3 Suspend: 350mA	+5V DC +/- 5% Max: 2.2A Typical: 1.8A S3 Suspend: 350mA
Mechanical Specifications		
Dimensions	4.50 x 6.50 in. (115 x 165 mm)	
Weight	9.6 oz. (273 g) with heat sink 10.4 oz. (295 g) with optional fan	
PCB thickness	0.078 in. (1.98 mm)	

Table 1: EPX-C414 Specifications (Continued)

Model	EPX-C414-3825-0	EPX-C414-3845-0
Environmental Specifications		
Temperature	-40 to +85°C (-40 to +185°F) (200 LFM airflow) -40 to +80°C (-40 to +176°F, still air)	-40 to +85°C (-40 to +185°F) (200 LFM airflow) -40 to +70°C (-40 to +158°F, still air)
Humidity (RH)	5% to 95% non-condensing	
Mechanical shock testing	MIL-STD-202G, Method 213B, Condition A 50g half-sine, 11 ms duration per axis, 3 axis	
Random vibration testing	MIL-STD-202G, Method 214A, Condition D .1g/Hz (11.95g rms), 20 minutes per axis, 3 axis	
RoHS compliant	Yes	
Operating Systems		
Runs 32/64-bit Windows, Linux, and other x86-compatible operating systems.		

Additional Accessories

Standoff kits are available and recommended for use with the EPX-C414.

- KIT-PCM-STANDOFF-4: Four piece nylon hex PC/104 standoff kit
- KIT-PCM-STANDOFF-B-4: Four piece brass hex PC/104 standoff kit

The following table lists the items contained in each kit.

Table 2: Standoff Kits

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. nylon hex PC/104 standoff kit	Standoff	Nylon 0.25” hex, 0.600” long male/female 4-40	4
	Hex nut	Hex nylon 4-40	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4
KIT-PCM-STANDOFF-B-4 4 pc. brass hex PC/104 standoff kit	Standoff	Brass 5 mm hex, 0.600” long male/female 4-40	4
	Hex nut	4-40 x 0.095 thick, nickel finish	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4

7. Configuration

This section describes the EPX-C414 components and configuration.

7.1 Component Layout

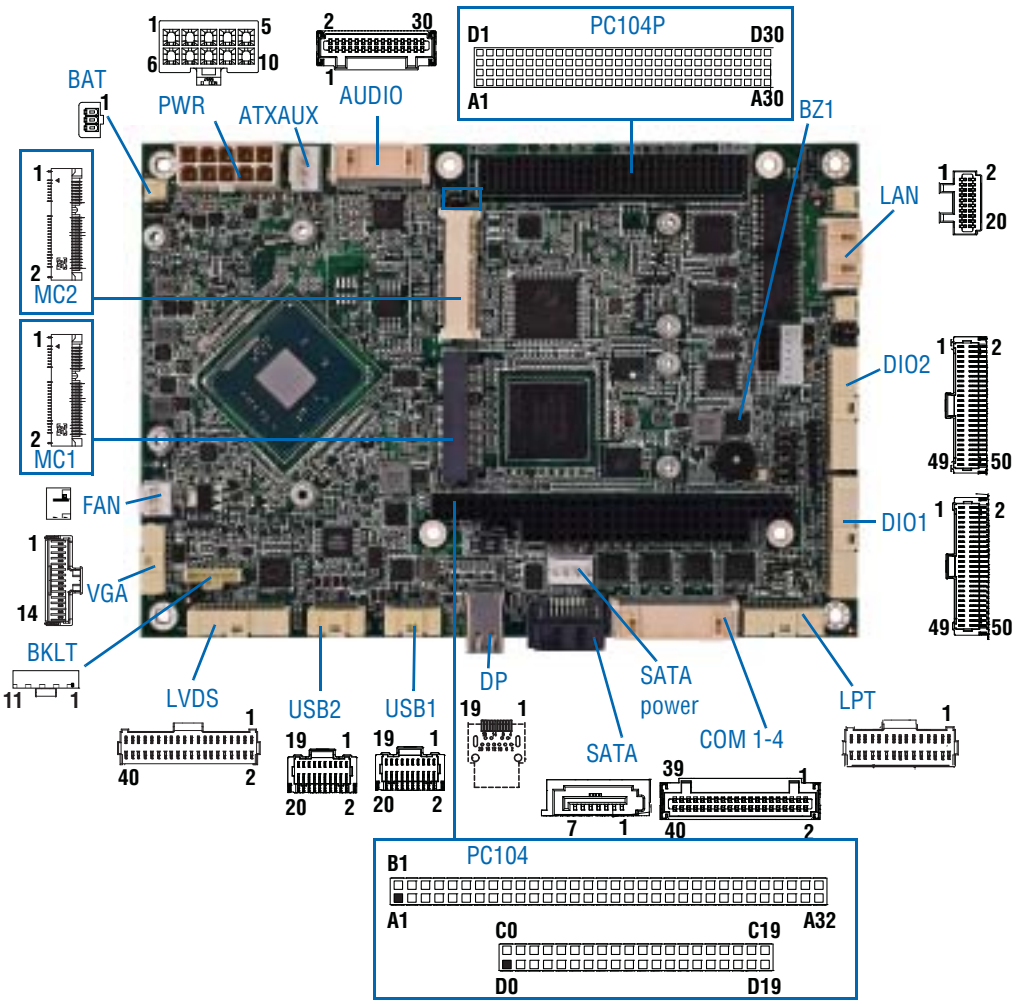
The EPX-C414 provides components on the top and bottom of the board.

7.1.1 Top View

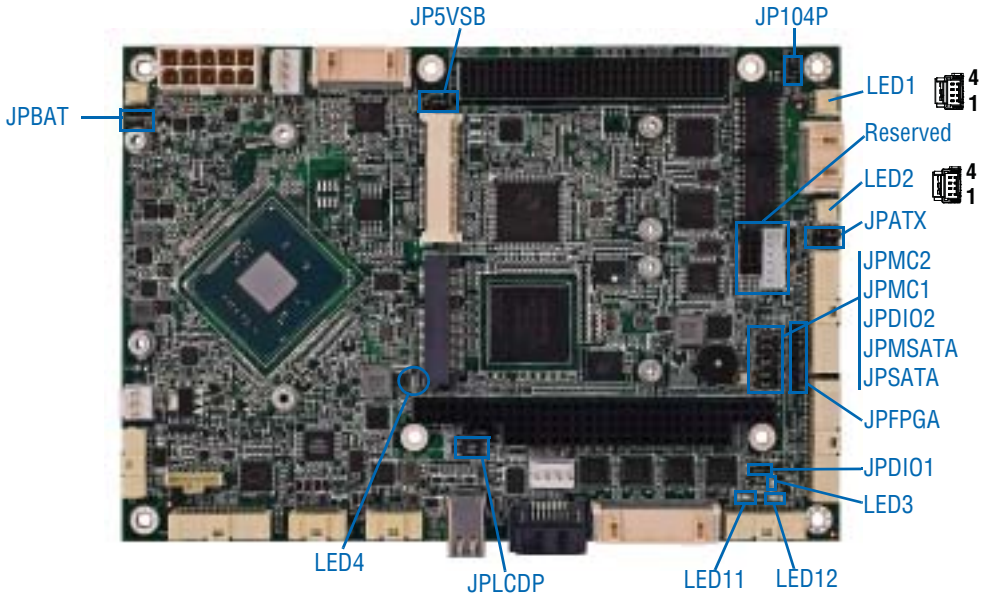
Table 3: Top View Components

Item	Description	Reference
PWR	Power and reset	page 21
JPATX	Power supply selection: AT or ATX-type power supply	page 46
AUDIO	HD audio connector	page 29
LED	LED1 and LED2 Ethernet LEDs	page 48
LED4	Status LED (on during boot process)	page 50
LED3, 12	Power LEDs	page 50
LED11	SATA LED	page 51
LAN	LAN Ethernet port	page 36
DIO	DIO1 and DIO2 digital input/output ports	page 37
LPT	Parallel printer port connector	page 25
COM 1-4	COM 1-4 serial connector	page 31
SATA	Serial ATA	page 34
DP	DisplayPort (Mini DP)	page 28
USB	USB1, USB2 ports	page 33
LVDS	LVDS Connector	page 27
VGA	Analog VGA connector	page 26
FAN	Fan power connector	page 23
BAT	External battery connector	page 23
BKLT	Backlight power connector	page 28
JPDIO	JPDIO1 and JPDIO2 digital power indicators	page 47
PC104	PC/104 bus connector	page 39
PC104P	PC/104-Plus bus connector	page 41
BZ1	BZ1 speaker	page 31
JPBAT	RTC battery enable	page 47
JP5VSB	5V standby power select	page 47
JP104P	PCI-104 power source select	page 47
JPFPGA	JTAG programming header for FPGA config EEPROM	page 48
JPMC	JPMC1 and JPMC2 MiniPCie	page 48

Connectors, top view



Jumpers and LEDs, top view

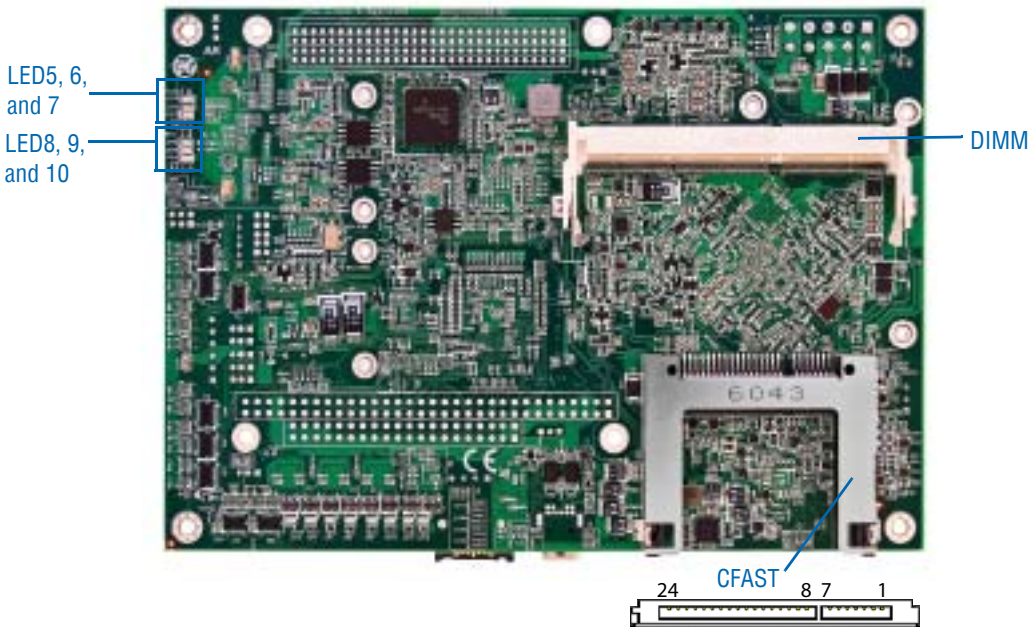


7.1.2 Bottom View

There are two Ethernet controllers on the EPX-C414 board. On the top side of the board, two headers (LED1 and LED2) drive remotely mounted LEDs or other inputs. Each controller has three LEDs on the bottom of the board to indicate connectivity status.

Table 4: Bottom View Components

Item	Description	Reference
LED 5, 6, and 7	Ethernet LED (activity, speed 100, speed 1000)	page 48
LED8, 9, and 10	Ethernet LED (activity, speed 100, speed 1000)	
CFAST	CFAST small form factor SATA SSD connector	page 35
DIMM	8 GB DDR3 SODIMM socket	page 35



7.2 I/O Port Map

The following tables list the EPX-C414 I/O ports.

NOTE The EPX-C414 uses a PnP BIOS resource allocation. Take care to avoid contention with resources allocated by the BIOS.

Table 5: Movable I/O Ranges

Device	Size (bytes)	Target
ACPI power management (PCU)	128	ACPI_BASE_ADDR (PM1BLK): PCI[B:0, D:31, F:0] + 40h
SMBus (PCU)	32	SMBA: PCI[B:0, D:31, F:3] + 20h
GPIO (PCU)	256	GBA: PCI[B:0, D:31, F:0] + 48h
RCBA (PCU)	1024	RCRB_BA: PCI[B:0, D:31, F:0] + F0h

Table 6: PCU Fixed I/O Addresses

I/O Address	Device
0000h-001Fh	DMA controller 82C37
0020h-0021h	Interrupt controller PIC 8259
0024h-0025h	Interrupt controller
0028h-0029h	Interrupt controller
002Ch-002Dh	Interrupt controller
002Eh-002Fh	Forward to Super I/O
0030h-0031h	Interrupt controller
0034h-0035h	Interrupt controller
0038h-0039h	Interrupt controller
003Ch-003Dh	Interrupt controller
0040h-0043h	Timer counter 8254
004Eh-004Fh	Forward to Super I/O
0050h-0053h	Timer counter 8254
0060h	Keyboard data port
0061h	NMI controller
0062h	8051 download 4K address counter
0064h	Keyboard status port
0066h	8051 download 8-bit data port
0070h-0077h	RTC controller
0080h-0091h	DMA controller
0092h	Reset generator
0093h-009Fh	DMA controller
00A0h-00A1h	Interrupt controller PIC 8259
00A4h-00A5h	Interrupt controller

Table 6: PCU Fixed I/O Addresses (Continued)

I/O Address	Device
00A8h-00A9h	Interrupt controller
0ACh-00ADh	Interrupt controller
00B0h-00B1h	Interrupt controller
00B2h-00B3h	Power management
00B4h-00B5h	Interrupt controller
00B8h-00B9h	Interrupt controller
00C0h-00DFh	DMA controller 82C37
00F0h	FERR#/IGNNE/interrupt controller
0120h-012Fh	Digital I/O (default)
0140h-01FFh	Reserved
0170h-0177h	IDE1 controller
0180h-01FFh	Reserved
0210h-0213h	SRAM control
0298h-029Bh	Reserved for Super I/O configuration
029Ch	Interrupt status register
029Dh	Status LED register
029Eh-029Fh	Watchdog timer control
02E8h-02EFh	COM4 (default)
02F8h-02FFh	COM2 (default)
0340h-03E7h	Reserved
0376h	IDE1 controller
0378h-037Bh	LPT (default)
03E8h-03EFh	COM3 (default)
03F0h-03F5h	Reserved
03F6h	IDE0 controller
03F8h-03FFh	COM1 (default)
04D0h-04D1h	Interrupt controller
0564h-0568h	Advanced watchdog
0CF9h	Reset generator

7.3 Interrupt Map

Hardware Interrupts (IRQs) are supported for both PC/104 (ISA), PCI and PCIe devices. Reserve IRQs in the BIOS CMOS configuration for use by legacy devices. The PCIe/PnP BIOS uses unreserved IRQs when allocating resources during the boot process. The table below lists IRQ resources as used by the EPX-C414.

Table 7: IRQ Resources

IRQ	Device
IRQ0	18.2 Hz heartbeat
IRQ1	Keyboard
IRQ2	Chained to slave controller (IRQ9)
IRQ3	COM2 *
IRQ4	COM1 *
IRQ5	COM3 *
IRQ6	COM4 *
IRQ7	LPT *
IRQ8	Real time clock
IRQ9	FREE **
IRQ10	Digital I/O
IRQ11	PCI interrupts
IRQ12	Mouse
IRQ13	Floating point processor
IRQ14	IDE
IRQ15	IDE

* These IRQ references are default settings that can be changed by the user in the CMOS Settings utility. Reference the Super I/O Control section under Intel.

** IRQ9 is commonly used by ACPI when enabled and may be unavailable (depending on operating system) for other uses.

*** IRQ15 is currently unavailable under the Windows operating systems.

Some IRQs can be freed for other uses if the hardware features they are assigned to are not being used. To free an interrupt, use the CMOS setup screens to disable any unused board features or their IRQ assignments.

Table 8: Interrupt Status Register - 29CH

Bit	Name
Bit 0	COM1
Bit 1	COM2
Bit 2	COM3
Bit 3	COM4
Bit 4	N/A
Bit 5	N/A
Bit 6	N/A
Bit 7	N/A
WinSystems does not provide software support for implementing the Interrupt Status Register to share interrupts. Some operating systems, such as Windows XP and Linux, have support for sharing serial port interrupts and examples are available. The user must implement the appropriate software to share interrupts for the other devices.	

7.4 PCI Devices and Functions

Table 9: Internal Devices

Bus	Device	Function	Device ID	Device/Function Description
0	0	0	0F00h	Device: SoC transaction router
0	2	0	0F31h	Device: Graphics and display
0	19	0	0F20h (IDE) 0F21h (IDE) 0F22h (AHCI) 0F23h (AHCI)	Device: SATA
0	26	0	0F18h	Device: Trusted execution engine
0	27	0	0F04h	Device: HD audio
0	28	0	0F48h	Device: PCI Express*
				Function: Root port 1
		1	0F4Ah	Device: PCI Express*
				Function: Root port 2
		2	0F4Ch	Device: PCI Express*
				Function: Root port 3
		3	0F4Eh	Device: PCI Express*
				Function: Root port 4
0	29	0	0F34h	Device: EHCI USB
0	31	0	0F1Ch	Device: Platform controller unit
				Function: LPC: Bridge to Intel legacy block
0	31	3	0F12h	Device: Platform controller unit
				Function: SMBus port

Table 10: External Devices

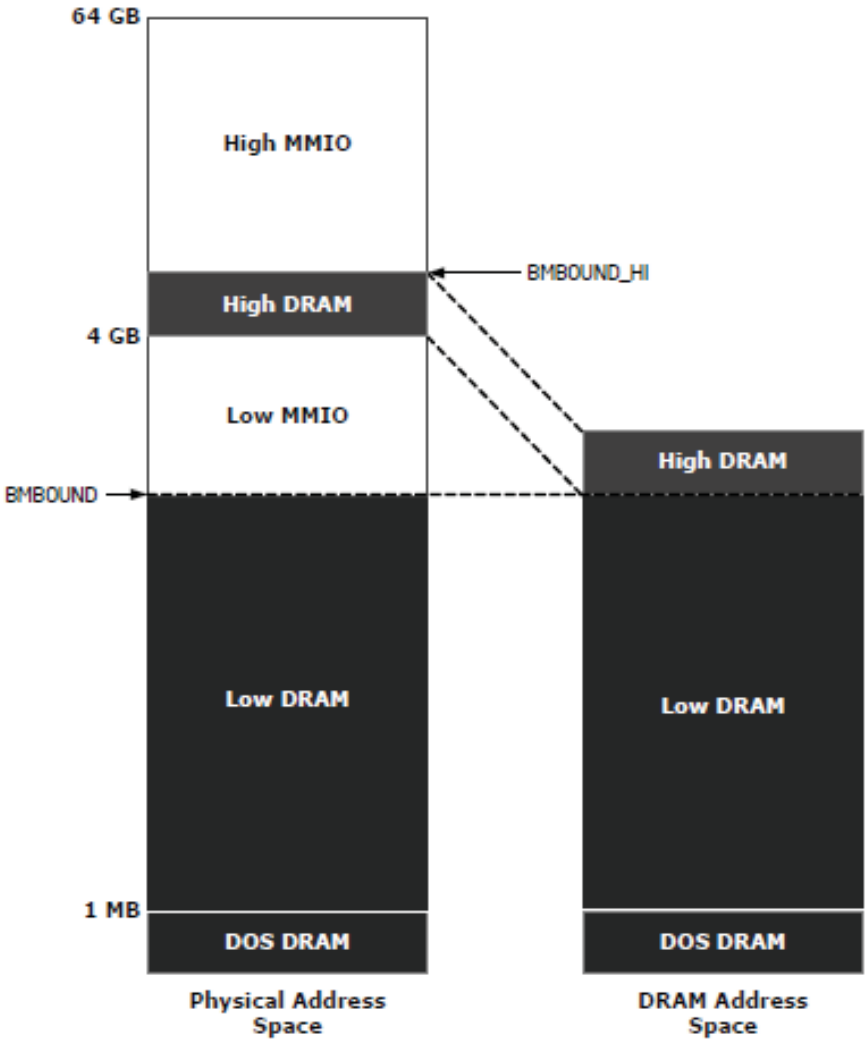
Bus	Device	Function	Device ID	Device/Function Description
3	0	0	104Ch	Device: 8240
				Function: PCI/PCI bridge
5	0	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
6	1	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
6	2	0	12D8h	Device: 2304
				Function: PCI/PCI bridge
7	0	0	8086h	Device: 8086
				Function: Intel Ethernet controller
8	0	0	8086h	Device: 8086
				Function: Intel Ethernet controller

7.5 DOS Legacy Memory Map

Table 11: HEX Ranges

HEX Range	Usage
0000:0000-0009:FFFF	Main memory (DOS area)
000A:0000-000B:FFFF	Legacy video area (SMM memory)
000C:0000-000D:FFFF	Expansion area
000E:0000-000E:FFFF	Extended system BIOS (lower)
000F:0000-000F:FFFF	System BIOS (upper)
0010:0000-TOM (top of memory)	Main memory
FEC0:0000-FEC7:FFFF	I/O APIC
FED0:x000-FED0:x3FF	High-precision event timers

7.5.1 Physical Address Space: DRAM and MMIO



7.6 Digital I/O Register Definitions

The EPX-C414 uses the WinSystems exclusive application-specific integrated circuit (ASIC), the WS16C48. This device provides 48 lines of digital I/O. There are 16 unique registers within the WS16C48. The following table summarizes the registers.

Table 12: Register definitions

I/O Address Offset	Page 0	Page 1	Page 2	Page 3
00h	Port 0 I/O	Port 0 I/O	Port 0 I/O	Port 0 I/O
01h	Port 1 I/O	Port 1 I/O	Port 1 I/O	Port 1 I/O
02h	Port 2 I/O	Port 2 I/O	Port 2 I/O	Port 2 I/O
03h	Port 3 I/O	Port 3 I/O	Port 3 I/O	Port 3 I/O
04h	Port 4 I/O	Port 4 I/O	Port 4 I/O	Port 4 I/O
05h	Port 5 I/O	Port 5 I/O	Port 5 I/O	Port 5 I/O
06h	Int_Pending	Int_Pending	Int_Pending	Int_Pending
07h	Page/Lock	Page/Lock	Page/Lock	Page/Lock
08h	Reserved	Pol_0	Enab_0	Int_ID0
09h	Reserved	Pol_1	Enab_1	Int_ID1
0Ah	Reserved	Pol_2	Enab_2	Int_ID2

The following sections provide details on each of the internal registers.

7.6.1 Port 0 through 5 I/O

Each I/O bit in each of the six ports can be individually programmed for input or output. Writing a 0 to a bit position causes the corresponding output pin to go to a high-impedance state (pulled high by external 10 kΩ resistors), allowing it to be used as an input. When used in the input mode, a read reflects the inverted state of the I/O pin, such that a high on the pin reads as a 0 in the register. Writing a 1 to a bit position causes that output pin to sink current (up to 12 mA), effectively pulling it low.

7.6.2 INT_PENDING

This read-only register reflects the combined state of the INT_ID0 through INT_ID2 registers. When any of the lower three bits are set, it indicates that an interrupt is pending on the I/O port corresponding to the bit position(s) that are set.

Reading this register allows an interrupt service routine to quickly determine if any interrupts are pending, and which I/O port has a pending interrupt.

7.6.3 PAGE/LOCK

This register serves two purposes. The upper two bits (D6 and D7) select the register page in use. Bits 0-5 allow the I/O ports to be locked. Write a 1 to the I/O port position to prohibit further writes to the corresponding I/O port.

Table 13: Page bits

Page	D7	D6	D5-D0
Page 0	0	0	1/0
Page 1	0	1	1/0
Page 2	1	0	1/0
Page 3	1	1	1/0

7.6.4 POL0 through POL2

These registers are accessible when Page 1 is selected. They allow interrupt polarity selection on a port-by-port and bit-by-bit basis. Writing a 1 to a bit position selects the rising edge detection interrupts. Writing a 0 to a bit position selects falling edge detection interrupts.

7.6.5 ENAB0 through ENAB2

These registers are accessible when Page 2 is selected. They allow for port-by-port and bit-by-bit enabling of the edge detection interrupts. When set to a 1, the edge detection interrupt is enabled for the corresponding port and bit. When cleared to 0, the bit's edge detection interrupt is disabled. Note that this register can be used to individually clear a pending interrupt by disabling and re-enabling the pending interrupt.

7.6.6 INT_ID0 through INT_ID2

These registers are accessible when Page 3 is selected. They are used to identify currently pending edge interrupts. A bit, when read as a 1, indicates that an edge of the polarity programmed into the corresponding polarity register has been recognized. Note that a write to this register (value ignored) clears ALL the pending interrupts in this register.

7.7 1 MB SRAM Registers

The EPX-C414 board provides 1 MB of battery-backed user SRAM. The 1 MB SRAM is normally used as a solid-state disk device by configuring appropriate driver for your operating systems.

For example, the DOS driver USSD.SYS can be used to make the SRAM appear as a drive in the system by adding the following to config.sys.

Device = `c:\ussd.sys /mod:u /pad:210 /dsz:1024`

The base address for the SRAM is located at 0210h.

There are four I/O registers used for accessing the memory array. The register definition and usage is defined below.

Table 14: Offset 0

OFFSET 0 - MSB Address Register
D7 - A23 of access address
D6 - A22 of access address
D5 - A21 of access address
D4 - A20 of access address
D3 - A19 of access address
D2 - A18 of access address
D1 - A17 of access address
D0 - A16 of access address

This register is write-only and holds the upper 8 bits of the 24-bit address used to access the 1 MB SRAM.

Table 15: Offset 1

OFFSET 1 - NSB Address Register
D7 - A15 of access address
D6 - A14 of access address
D5 - A13 of access address
D4 - A12 of access address
D3 - A11 of access address
D2 - A10 of access address
D1 - A9 of access address
D0 - A8 of access address

This register is write-only and holds the middle 8 bits of address used to access the 1 MB memory array. Writing this register also clears the LSB address counter to 0.

Table 16: Offset 2

OFFSET 2 - Data Access Register A
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is the primary window to the memory array. A value written to this port is written to the address in the memory array specified by the MSB register, the

NSB register, and the current LSB counter address. In like fashion, a read from this I/O address results in the current memory array data at the address specified by the MSB register, the NSB register, and the LSB address counter.

In either case, read or write, an access to this register results in the LSB address counter being incremented immediately following the access so that the next access is at the next sequential address in the array. This incrementing process does not carry into the NSB or MSB register which must be rewritten every 256 bytes.

Table 17: Offset 3

OFFSET 3 - Data Access Register B
D7 - D7 of memory data
D6 - D6 of memory data
D5 - D5 of memory data
D4 - D4 of memory data
D3 - D3 of memory data
D2 - D2 of memory data
D1 - D1 of memory data
D0 - D0 of memory data

This read/write register is used to access the memory array when post incrementing of the LSB counter is not desired. The byte written or read is still specified by the 24-bit combination of the MSB register, the NSB register, and the LSB counter. However, the LSB counter is not altered following the access. It is then necessary to do one more read from Data Access Register A to bump the address to the next byte.

Table 18: Offset 4

OFFSET 4 - Write Protect Register
D7 - D6 - Reserved
D0 - Write Protect Bit, 0 = Protected, 1 = Writeable

This write-only register controls the write protect function of the 1 MB SRAM board. On power up, the write protect bit is cleared (disabling writes) and must be explicitly enabled by writing a 1 to the I/O port at the BASE address +4. To re-enable the write protection, write a 0 at this register. The USSD.SYS device enables writing only during that time when a sector is being transferred, which contributes greatly to data safety and integrity.

7.8 Watchdog Timer Registers

The EPX-C414 features an advanced watchdog timer to guard against software lockups; it resets the system if software does not pet the watchdog within the given time-out period. Enable and boot times are selectable from the CMOS setup.

Two interfaces are provided to the watchdog timer. The Advanced interface is the most flexible and recommended for new designs. The other interface option is provided for software compatibility with older WinSystems single-board computers.

7.8.1 Advanced

Enable the watchdog timer in the BIOS settings by entering any non-zero value for Watchdog Timeout on the Intel Super I/O Control screen. A non-zero value represents the number of minutes prior to reset during system boot. When the operating system is loaded, the watchdog can be disabled or reconfigured in the application software.

NOTE WinSystems recommends using a long timeout if the watchdog is enabled when trying to boot any operating system.

The watchdog can be enabled, disabled, or reset by writing the appropriate values to the configuration registers located at I/O addresses 565h and 566h. The watchdog is enabled by writing a non-zero timeout value to the I/O address 566h, and is disabled by writing 00h to the same address. The watchdog timer is serviced by writing the desired timeout value to I/O port 566h. If the watchdog has not been serviced within the allotted time, the circuit resets the CPU.

The timeout value can be set to anywhere from 1 second to 255 minutes. If port 565h bit 7 equals 0, the timeout value written into I/O address 566h is in minutes. If port 565 bit 7 equals 1, the timeout value written to address 566h is in seconds.

Table 19: Watchdog Timer Examples

Port Address	Port Bit 7 Value	Port Address	Value	Reset Interval
565h	x	566h	00h	DISABLED
565h	1	566h	03h	3 seconds
565h	1	566h	1Eh	30 seconds
565h	0	566h	04h	4 Minutes
565h	0	566h	05h	5 Minutes
Software watchdog timer PET = PORT 566h, write the timeout value.				

7.8.2 Standard

Standard requires changing the default I/O ranges within the BIOS.

The watchdog can be enabled or disabled via software by writing an appropriate timeout value to I/O port 29EH. See the table below.

Table 20: Timeout Values

Port Address	Value	Reset Interval
29EH	00h	DISABLED
	01h	3 SECONDS
	03h	30 SECONDS
	05h	300 SECONDS
29FH	ANY	RESET TIMER

7.9 Real-time Clock/Calendar

A real-time clock is used as the AT-compatible clock/calendar. It supports a number of features including periodic and alarm interrupt capabilities. In addition to the time and date-keeping functions, the system configuration is kept in CMOS RAM contained within the clock section. A battery must be enabled for the real-time clock to retain time and date during a power down.

7.10 Connectors

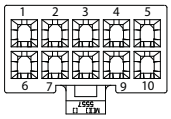
7.10.1 PWR Power and Reset

Power is applied to the EPX-C414 via the connector at PWR. DC 5V is the main supply to the board. The +12V and -12V DC are not required for the basic SBC operation, this supplies the PC104, PC/104-Plus, and backlight connectors.

A jumper is provided to short 5V and 5V Stand_by. This is used when an AT power supply is connected to the system and pin 6 of PWR connector is open (not connected to +5V).

WinSystems offers the cable CBL-265-G-2-1.5 to simplify this connection.

Layout and Pin Reference

Pin	Name	Pin	Name
			
1	PSON	6	+5VSB
2	GND	7	+5V
3	GND	8	+5V
4	+12VDC	9	-12V
5	+3.3V*	10	GND
*3.3V only connects to PC/104-*Plus* connector*			

Connector

MOLEX 87427-1043 (PWR) (2x5, 4.2 mm locking header)

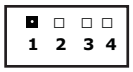
Matching Connectors

- MOLEX 39-01-2105 (housing)
- MOLEX 39-00-0039 (crimp)

7.10.2 ATXAUX ATX Signals Connector

ATX signals for the power button, reset and power good are provided at ATXAUX. WinSystems offers the cable CBL-265-G-2-1.5 to simplify this connection.

Layout and Pin Reference

Pin	Name
	
1	RESET
2	GND
3	PWRBTN
4	PWRGOOD

Connector

MOLEX 22-11-2042 (ATXAUX)

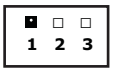
Matching Connectors

- MOLEX 39-01-2105 (housing)
- MOLEX 08-55-0101 (crimp)

7.10.3 FAN Fan Power Connector

A 3-pin connector is provided for power and control of a CPU fan. On-board circuitry is provided to monitor the CPU temperature and control the fan appropriately. The fan connector uses a Molex 22-11-2032 mating connector.

Layout and Pin Reference

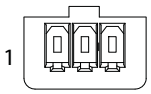
Pin	Name
	
1	TACH
2	VDD
3	GND

7.10.4 BAT External Battery Connector

An optional external battery, connected at BAT, supplies the EPX-C414 board with standby power for the real-time clock, and CMOS setup RAM and SRAM (applicable models only). An extended temperature lithium battery is available from WinSystems, part number BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2.

A power supervisory circuit contains the voltage sensing circuit and an internal power switch to route the battery or standby voltage to the circuits selected for backup. The battery automatically switches ON when the V_{CC} of the systems drops below the battery voltage and back OFF again when V_{CC} returns to normal.

Layout and Pin Reference

Pin	Name
	
1	GND
2	VBAT
3	NC (no connect)

WARNING: BAT-LTC-E-36-16-2 or BAT-LTC-E-36-27-2 must be connected at BAT. Improper installation of the battery could result in explosive failure. Please be careful to note correct connection at location BAT.

Connector

MOLEX 501953-0307 (BAT)

Matching Connectors

- MOLEX 501939-0300 (housing)
- MOLEX 501334-0100 OR 501334-0000 (crimp)

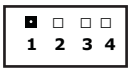
WinSystems battery BAT-LTC-E-36-16-2 and BAT-LTC-E-36-27-2 simplify these connections to the board.

BAT-LTC-E-36-16-2

BAT-LTC-E-36-27-2

7.10.5 SATA PWR SATA Power Connector

Layout and Pin Reference

Pin	Name
	
1	+5V
2	GND
3	GND
4	+12V

Connector

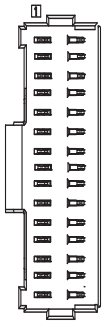
MOLEX 22-11-2042 (SATA PWR)

Matching Connectors

- MOLEX 39-01-2105 (housing)
- MOLEX 08-55-0101 (crimp)

7.10.6 LPT Parallel Printer Port Connector

Layout and Pin Reference

	Pin	Name	Pin	Name
	1	GND	2	GND
	3	STROBE	4	AUTOFEED
	5	DATA0	6	ERROR
	7	DATA1	8	PRINTER_INT
	9	DATA2	10	SELECT
	11	DATA3	12	GND
	13	DATA4	14	GND
	15	DATA5	16	GND
	17	DATA6	18	GND
	19	DATA7	20	GND
	21	ACK	22	GND
	23	BUSY	24	GND
	25	PAPER_END	26	GND
	27	SELECT	28	GND
	29	GND	30	GND

Additional Information

The LPT port, located at LPT, is a multimode parallel printer port that supports the PS/2 Standard Bidirectional Parallel Port (SPP) and Enhanced Parallel Port (EPP) functionality.

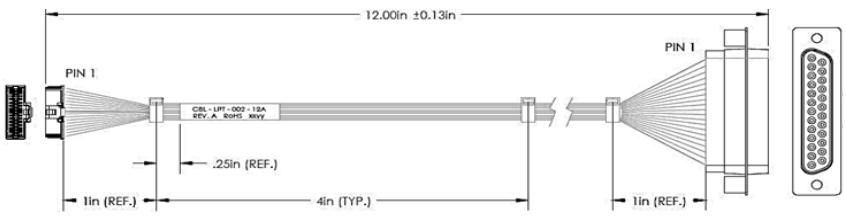
The printer port can also be used as two additional general-purpose I/O ports if a printer is not required. The first port is configured as eight, either input or output-only, lines. The other port is configured as five input and three output lines.

Connector

MOLEX 501571-3007 (LPT)

Matching Connectors

- MOLEX 501189-3010 (housing)
- MOLEX 501193-2000 (crimp)

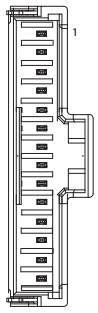


CBL-LPT-002-12

7.10.7 VGA Analog VGA Connector

NOTE The EPX-C414 has one VGA, one DisplayPort, and one low-voltage differential signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference

	Pin	Name	Description
	1	RED	Red signal input
	2	GND	GND
	3	GREEN	Green signal input
	4	GND	GND
	5	BLUE	Blue signal input
	6	GND	GND
	7	HSYNC	Horizontal synchronization
	8	GND	GND
	9	VSYNC	Vertical synchronization
	10	GND	GND
	11	SDA	Data (synchronized)
	12	GND	GND
	13	SCL	Clock (synchronizes data)
	14	V_{CC}	5V input

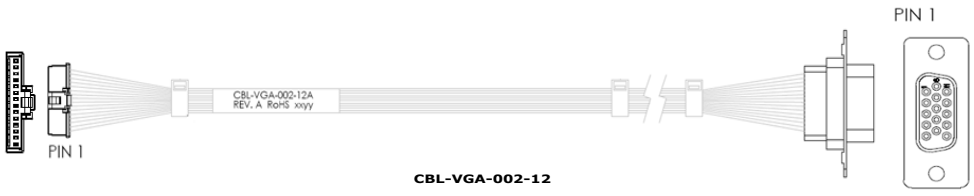
Connector

MOLEX 501568-1407 (VGA)

Matching Connectors

- MOLEX 501330-1400 (housing)
- MOLEX 501334-0000 (crimp)

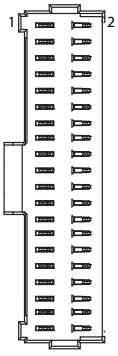
WinSystems offers CBL-VGA-002-12, to interface with an LCD panel.



7.10.8 LVDS Connector

NOTE The EPX-C414 has one VGA, one DisplayPort, and one low-voltage differential signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference



Pin	Name	Pin	Name
1	SWVDD	2	GND
3	DA0-	4	DA0+
5	DA1-	6	DA1+
7	SWVDD	8	GND
9	DA2-	10	DA2+
11	DA3-	12	DA3+
13	SWVDD	14	GND
15	ACLK-	16	ACLK+
17	DDC_CLK	18	GND
19	DDC_DATA	20	GND
21	SWVDD	22	GND
23	DB0-	24	DB0+
25	DB1-	26	DB1+
27	SWVDD	28	GND
29	DB2-	30	DB2+
31	DB3-	32	DB3+
33	SWVDD	34	GND
35	BCLK-	36	BCLK+
37	NC	38	GND
39	NC	40	GND

Additional Information

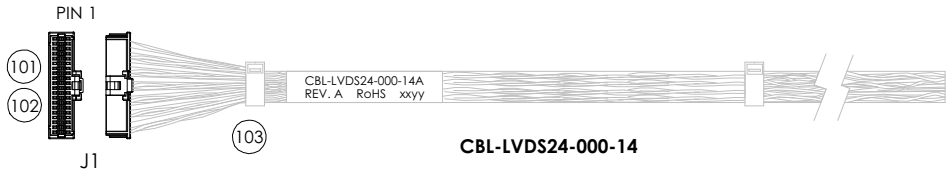
See “JPLCDP Panel Power Jumper” on page 45 for information on supplying power to LVDS. WinSystems offers CBL-LVDS24-000-14 for the LVDS interface.

Connector

MOLEX 501571-4007 (LVDS)

Matching Connectors

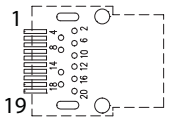
- MOLEX 501189-4010 (housing)
- MOLEX 501193-2000 (crimp)



7.10.9 DP DisplayPort (Mini DP)

NOTE The EPX-C414 has one VGA, one mini DisplayPort, and one low-voltage differential signaling (LVDS) interface. Only two of the three outputs may be active simultaneously.

Layout and Pin Reference



Pin	Name	Pin	Name
1	ML_LANE0 (P)	2	GND
3	ML_LANE0 (N)	4	ML_LANE1 (P)
5	GND	6	ML_LANE1 (N)
7	ML_LANE2 (P)	8	GND
9	ML_LANE2 (N)	10	ML_LANE3 (P)
11	GND	12	ML_LANE3 (N)
13	CONFIG1	14	CONFIG2
15	AUXCH (P)	16	GND
17	AUXCH (N)	18	HOTPLUG
19	RETURN	20	DP_PWR

Pins 13 and 14 may either be directly connected to ground or connected to ground through a pull-down resistor.

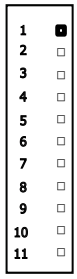
See “JPLCDP Panel Power Jumper” on page 45 for information on supplying power to DP.

Connector

Adam-Tech MDPC-S-RA or equivalent

7.10.10 BKLT Backlight Power Connector

Layout and Pin Reference



Pin	Name	Description
1	+5VDC	
2	LBKLT_EN-	Low active backlight enable
3	LBKLT_EN+	High active backlight enable
4	GND	Ground
5	+12VDC	
6	PWM	
7	NC	No connect
8	NC	
9	NC	
10	LCTL_B DATA	
11	LCTL_A CLK	

HAZARD WARNING: LCD panels can require a high voltage for the panel backlight. This high-frequency voltage can exceed 1000 Volts and can present a shock hazard. Care should be taken when wiring and handling the inverter output. To avoid the danger of shock and to avoid the panel, make all connection changes with the power removed.

Connector

MOLEX 501131-1107 (BKLT)

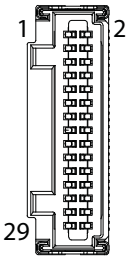
Matching Connectors

- MOLEX 501330-1100 (housing)
- MOLEX 501334-0000 (crimp)

WinSystems backlight cables are panel specific. Please contact an Application Engineer through technical support for details (see the “Introduction” on page 1 for details).

7.10.11 AUDIO HD Audio Connector

Layout and Pin Reference

	Pin	Name	Pin	Name
	1	OUT_R	2	MIC1_R
	3	OUT_L	4	MIC1_L
	5	AUDIO_GND	6	AUDIO_GND
	7	SUR_R	8	MIC2_R
	9	SUR_L	10	MIC2_L
	11	AUDIO_GND	12	AUDIO_GND
	13	CENTER	14	LINE_R
	15	LFE	16	LINE_L
	17	AUDIO_GND	18	AUDIO_GND
	19	SIDE_R	20	CD_R
	21	SIDE_L	22	CD_L
	23	AUDIO_GND	24	CD_GND
	25	HEAD_R	26	AUDIO_GND
	27	HEAD_L	28	AUDIO_GND
	29	AUDIO_GND	30	AUDIO_GND

Additional Information

The Intel HD audio controller is included with a VIA 1708B codec.

Audio connection is provided at AUDIO. Three cables are available from WinSystems to adapt to this connector:

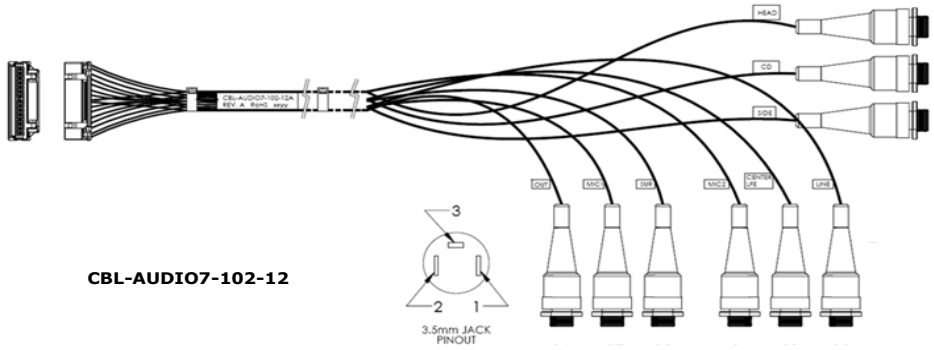
- CBL-AUDIO7-102-12 provides full 7.1 audio support.
- A simplified cable, CBL-AUDIO2-102-12, provides basic Line In, Line Out, and Microphone audio support.
- CBL-AUDIO5-102-12 provides 5.1 audio support.

Connector

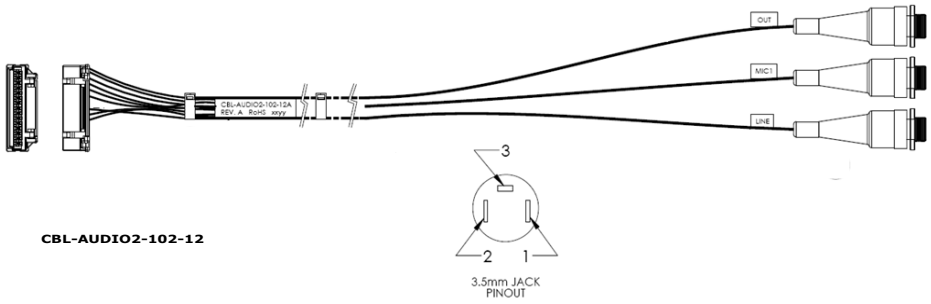
MOLEX 502046-3070 (AUDIO)

Matching Connectors

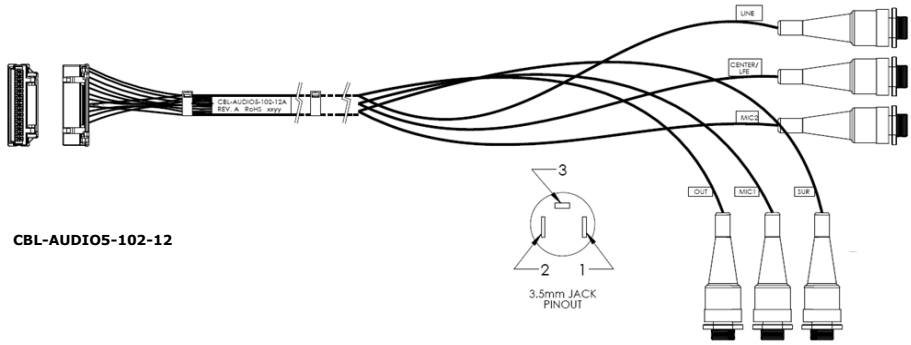
- MOLEX 503110-3000 (housing)
- MOLEX 501930-1100 (crimp)



CBL-AUDIO7-102-12



CBL-AUDIO2-102-12



CBL-AUDIO5-102-12

7.10.12 BZ1 Speaker

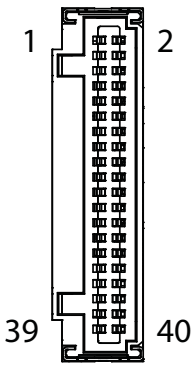
Speaker

An on-board speaker, BZ1, is available for sound generation. The BIOS activates the buzzer to beep during POST failure. Each error has its own unique beep code. Refer to InsydeH20 BIOS POST Tasks for details.

The board beeps once at power up, and beeps several times if there is no RAM.

7.10.13 SERIAL (COM 1 through COM4) Connector

Layout and Pin Reference



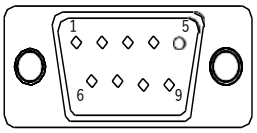
Pin	RS-232	RS-422	RS-485	Pin	RS-232	RS-422	RS-485
1	COM1_DCD	TX-	TX/RX-	2	COM1_DSR	–	–
3	COM1_RX	TX+	TX/RX+	4	COM1_RTS	–	–
5	COM1_TX	RX+	–	6	COM1_CTS	–	–
7	COM1_DTR	RX-	–	8	COM1_RI	–	–
9	GND	GND	GND	10	NC	NC	NC
11	COM2_DCD	TX-	TX/RX-	12	COM1_DSR	–	–
13	COM2_RX	TX+	TX/RX+	14	COM1_RTS	–	–
15	COM2_TX	RX+	–	16	COM1_CTS	–	–
17	COM2_DTR	RX-	–	18	COM1_RI	–	–
19	GND	GND	GND	20	NC	NC	NC
21	COM3_DCD	TX-	TX/RX-	22	COM1_DSR	–	–
23	COM3_RX	TX+	TX/RX+	24	COM1_RTS	–	–
25	COM3_TX	RX+	–	26	COM1_CTS	–	–
27	COM3_DTR	RX-	–	28	COM1_RI	–	–
29	GND	GND	GND	30	NC	NC	NC
31	COM4_DCD	TX-	TX/RX-	32	COM1_DSR	–	–
33	COM4_RX	TX+	TX/RX+	34	COM1_RTS	–	–
35	COM4_TX	RX+	–	36	COM1_CTS	–	–
37	COM4_DTR	RX-	–	38	COM1_RI	–	–
39	GND	GND	GND	40	NC	NC	NC

Additional Information

The FPGA code provides four 16C550-compatible serial ports through COM1 to COM4. All four ports are RS232 and RS422/RS485 configurable. The mode selection, RS485 flow control, and termination enable-selection are controlled through the FPGA, and user-selectable in the BIOS Setup Utility.

7.10.14 COM1, COM2, COM3, COM4 DB9 Male Connector

Layout and Pin Reference

	Pin	RS-232	RS-422	RS-485
	1	DCD	TX-	TX/RX-
	2	RX	TX+	TX/RX+
	3	TX	RX+	NA
	4	DTR	RX-	NA
	5	GND	GND	GND
	6	DSR	NA	NA
	7	RTS	NA	NA
	8	CTR	NA	NA
	9	RI	NA	NA

All ports are configured as data terminal equipment (DTE). Both the send and receive registers of each port have a 16-byte FIFO. All serial ports have 16C550-compatible UARTs. The RS-232 has a charge pump to generate the plus and minus voltages so the EPX-C414 only requires +5V to operate. An independent, software-programmable baud rate generator is selectable from 50 through 115.2 kbps. Individual modem handshake control signals are supported for all ports.

Connector

MOLEX 502046-4070 (serial)

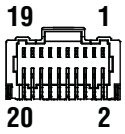
Matching Connectors

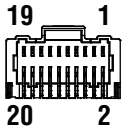
- MOLEX 503110-4000 (housing)
- MOLEX 501930-1100 (crimp)

7.10.15 USB1, USB2 - USB 2.0 Ports

Eight USB ports are supported through two on-board connectors. These ports have ESD suppression to provide increased robustness. Power these ports from the standby voltage rail to support a wake event.

Layout and Pin Reference

Pin	Name	Pin	Name
USB 1 			
1	USB0_PWR	2	USB1_PWR
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	USB_GND	8	USB_GND
9	USB_GND	10	USB_GND
11	USB_GND	12	USB_GND
13	USB2_PWR	14	USB3_PWR
15	USB2-	16	USB3-
17	USB2+	18	USB3+
19	USB_GND	20	USB_GND

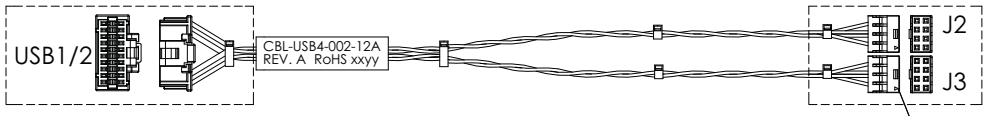
Pin	Name	Pin	Name
USB 2 			
1	USB4_PWR	2	USB5_PWR
3	USB4-	4	USB5-
5	USB4+	6	USB5+
7	USB_GND	8	USB_GND
9	USB_GND	10	USB_GND
11	USB_GND	12	USB_GND
13	USB6_PWR	14	USB7_PWR
15	USB6-	16	USB7-
16	USB6+	18	USB7+
19	USB_GND	20	USB_GND

Connector

MOLEX 501571-2007 (USB) Pico-clasp

Matching Connectors

- MOLEX 501189-2010 (housing)
- MOLEX 501193-2000 (crimp)



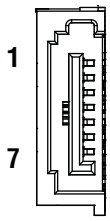
CBL-USB4-002-12

Up to two USB cables may be attached to the EPX-C414 via the connectors for a total of eight USB 2.0 ports. These are terminated to 20-pin connectors at USB1 and USB2. An adapter cable CBL-USB4-002-12 is available from WinSystems for connection along with ADP-IO-USB-001.

7.10.16 SATA Serial ATA (SATA)

The EPX-C414 supports one SATA interface, multiplexed with the CFast connector. Only one of these two features (either SATA or CFast) is available at a time.

Layout and Pin Reference

	Pin	Name
	1	GND
	2	A+
	3	A-
	4	GND
	5	B-
	6	B+
	7	GND

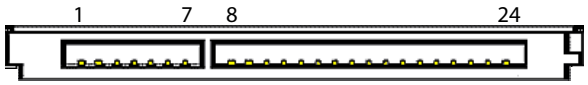
Connector

- MOLEX 67490-1220 (SATA) or equivalent
- 3M 5607-4200-SH 1x7, right angle

7.10.17 CFAST CFast Connector

CFast is a small form-factor SATA SSD standard that encompasses CFast data storage cards. This interface is multiplexed with the SATA connector. Only one of the two features is available at any time.

Layout and Pin Reference

Pin	Name	Pin	Name
			
1	GND	2	D3
3	D4	4	D5
5	D6	6	D7
7	HDCS0	8	GND
9	GND	10	GND
11	GND	12	GND
13	CFVCC	14	GND
15	GND	16	GND
17	GND	18	A2
19	A1	20	A0
21	D0	22	D1
23	D2	24	NC

Connector

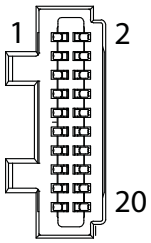
3M N7G24-A0B2EB-10-3WF or equivalent

7.10.18 DIMM 8 GB DDR3 SODIMM Socket

Connector DIMM is a SODIMM 204-pin DDR3-LV compatible socket, accommodating a maximum of 8 GB RAM.

7.10.19 LAN Ethernet Port

Layout and Pin Reference

	Pin	Name	Pin	Name
	1	(G1) MX1+	2	(G1) MX1-
	3	(G1) MX2+	4	(G1) MX2-
	5	(G1) MX3+	6	(G1) MX3-
	7	(G1) MX4+	8	(G1) MX4-
	9	GND	10	GND
	11	(G2) MX1+	12	(G2) MX1-
	13	(G2) MX2+	14	(G2) MX2-
	15	(G2) MX3+	16	(G2) MX3-
	17	(G2) MX4+	18	(G2) MX4-
	19	GND	20	GND

Additional Information

The EPX-C414 is equipped with two Intel i210 Gigabit Ethernet controllers. Each of these provides a standard IEEE 802.3 Ethernet interface for 1000/100/10BASE-T networks. The connections for each Ethernet port are available at LAN. WinSystems offers CBL-ENET2-002-12, to interface with two RJ-45 jacks.

On-board Ethernet activity LEDs LED5 - LED7 are provided for Port 1. LEDs LED8 - LED10 are associated with Port 2. These activity signals are also available off-board for enclosures or other applications that have remote mounting requirements. The activity signals for Port 1 are provided at connector LED1. The signals for Port 2 are provided at LED2. (See the LED tables for signal and pin definitions.) Three on-board LEDs are provided to give Ethernet channel status. Refer to “LED1, LED2 Ethernet LEDs” on page 48.

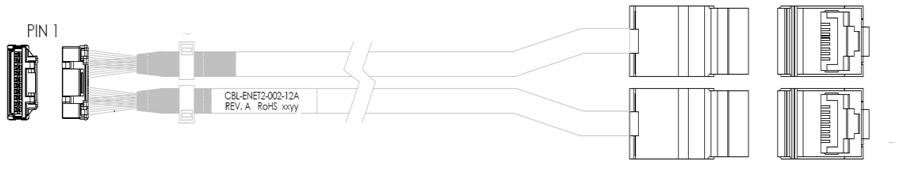
Connector

MOLEX 502046-2070 (LAN)

Matching Connectors

- MOLEX 503110-2000 (housing)
- MOLEX 501930-1100 (crimp)

WinSystems offers the CBL-ENET2-002-12 cable to simplify this connection.



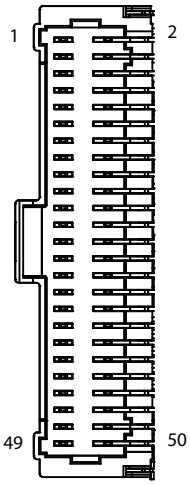
CBL-ENET2-002-12

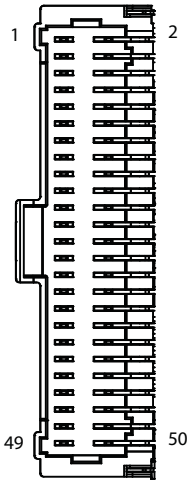
7.10.20 DIO1, DIO2 Digital Input/Output

The EPX-C414 has two digital I/O connectors to support 48 bi-directional TTL digital I/O lines, 24 of which are capable of event-sense interrupt generation. External voltage translators allow the signals to drive or sink up to 5VDC.

The 48 lines of digital I/O are terminated through two 50-pin connectors at DIO1 and DIO2. The DIO1 connector handles I/O ports 0 through 2 while DIO2 handles ports 3 through 5.

Layout and Pin Reference

	Pin	Name	Pin	Name
DIO1 	1	Bit C7	2	GND
	3	Port 2 Bit C6	4	GND
	5	Port 2 Bit C5	6	GND
	7	Port 2 Bit C4	8	GND
	9	Port 2 Bit C3	10	GND
	11	Port 2 Bit C2	12	GND
	13	Port 2 Bit C1	14	GND
	15	Port 2 Bit C0	16	GND
	17	Port 1 Bit B7	18	GND
	19	Port 1 Bit B6	20	GND
	21	Port 1 Bit B5	22	GND
	23	Port 1 Bit B4	24	GND
	25	Port 1 Bit B3	26	GND
	27	Port 1 Bit B2	28	GND
	29	Port 1 Bit B1	30	GND
	31	Port 1 Bit B0	32	GND
	33	Port 0 Bit A7	34	GND
	35	Port 0 Bit A6	36	GND
	37	Port 0 Bit A5	38	GND
	39	Port 0 Bit A4	40	GND
	41	Port 0 Bit A3	42	GND
	43	Port 0 Bit A2	44	GND
	45	Port 0 Bit A1	46	GND
	47	Port 0 Bit A0	48	GND
	49	+3.3/5V	50	GND

	Pin	Name	Pin	Name
DIO2 	1	Bit C7	2	GND
	3	Port 5 Bit C6	4	GND
	5	Port 5 Bit C5	6	GND
	7	Port 5 Bit C4	8	GND
	9	Port 5 Bit C3	10	GND
	11	Port 5 Bit C2	12	GND
	13	Port 5 Bit C1	14	GND
	15	Port 5 Bit C0	16	GND
	17	Port 4 Bit B7	18	GND
	19	Port 4 Bit B6	20	GND
	21	Port 4 Bit B5	22	GND
	23	Port 4 Bit B4	24	GND
	25	Port 4 Bit B3	26	GND
	27	Port 4 Bit B2	28	GND
	29	Port 4 Bit B1	30	GND
	31	Port 4 Bit B0	32	GND
	33	Port 3 Bit A7	34	GND
	35	Port 3 Bit A6	36	GND
	37	Port 3 Bit A5	38	GND
	39	Port 3 Bit A4	40	GND
	41	Port 3 Bit A3	42	GND
	43	Port 3 Bit A2	44	GND
	45	Port 3 Bit A1	46	GND
	47	Port 3 Bit A0	48	GND
	49	+3.3/5V	50	GND

Connector

MOLEX 501571-5007 (DIO1, DIO2) 2x25, 1mm box headers

7.10.21 PC104 PC/104 Bus

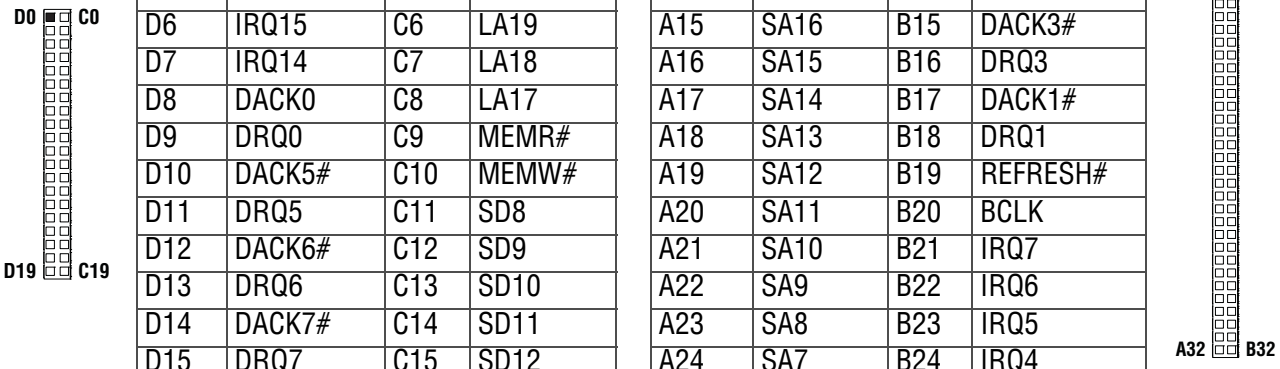
The PC/104 bus is electrically equivalent to the ISA bus and is generated from LPC by FPGA. Standard PC/104 I/O cards can be populated on EPX-C414's connectors, located at PC104. The interface does not support hot swap capability. The PC/104 bus connector pin definitions are provided below for reference. Refer to the PC/104 Bus Specification for specific signal and mechanical specifications.

This interface is PC/104 version 2.5 compliant.

Layout and Pin Reference

Pin	Name	Pin	Name
D0	GND	C0	GND
D1	MEMCS16#	C1	SBHE#
D2	IOCS16#	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0	C8	LA17
D9	DRQ0	C9	MEMR#
D10	DACK5#	C10	MEMW#
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5V	C16	SD13
D17	MASTER#	C17	SD14
D18	GND	C18	SD15
D19	GND	C19	KEY

Pin	Name	Pin	Name
A1	IOCHK#	B1	GND
A2	SD7	B2	RESET
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	NC
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	SRDY
A9	SD0	B9	+12V
A10	IOCHRDY	B10	KEY
A11	AEN	B11	SMEMW#
A12	SA19	B12	SMEMR#
A13	SA18#	B13	IOW#
A14	SA17	B14	IOR#
A15	SA16	B15	DACK3#
A16	SA15	B16	DRQ3
A17	SA14	B17	DACK1#
A18	SA13	B18	DRQ1
A19	SA12	B19	REFRESH#
A20	SA11	B20	BCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	IRQ6
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	DACK2#
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND



= Active low signal

Shaded cells indicate power pins.

Additional Information

1. Rows C and D are not required on 8-bit modules.
2. B10 and C19 are key locations. WinSystems uses key pins as connections to GND.
3. Signal timing and function are as specified in ISA specification.
4. Signal source/sink current differ from ISA values.

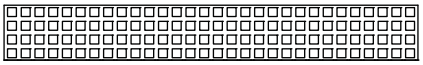
Connectors

- 64-Pin SAMTEC type ESQ-132-12-G-D or equivalent, solder-tail (short) pins
- 40-Pin SAMTEC type ESQ-12012-G-D or equivalent, solder-tail (short) pins

No keys in connector, and no cut pins.

7.10.22 PC104P PC/104-*Plus* Bus

Layout and Pin Reference

Pin	A	B	C	D
		D1 D30  A1 A30		
1	GND/5.0V KEY[2]	RESERVED	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0#	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1#	AD15	+3.3V
9	SERR#	GND	SB0#	PAR
10	GND	PERR#	+3.3V	SDONE
11	STOP#	+3.3V	LOCK#	GND
12	+3.3V	TRDY#	GND	DEVSEL#
13	FRAME#	GND	IRDY#	+3.3V
14	GND	AD16	+3.3V	C/BE2#
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3#	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0#	GND	REQ1#	VI/O
24	GND	REQ2#	+5V	GNT0#
25	GNT1#	VI/O	GNT2#	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD#	+5V	RST#
29	+12V	INTA#	INTB#	INTC#
30	-12V	REQ3#	GNT3#	GND/3.3V KEY[2]

= Active Low Signal

Shaded cells indicate power pins.

Additional Information

The PC/104-*Plus* is electrically equivalent to the 33 MHz PCI bus (and generated by the TI XIO2001 PCIe to PCI bridge chip) and terminated to a 120-pin non-stack-through connector. The input voltage of the connector can be configurable between 5VDC and 3.3VDC with a jumper. The interface does not support hot-swap capability.

The interface is PC104/Plus v2.0 compliant.

Connector

120-Pin SAMTEC type ESQT-130-G-Q-368, solder-tail (short) pins

7.10.23 MC1 and MC2 MiniPCI Express

The EPX-C414 includes MiniPCIe sockets at MC1 and MC2.

These support a variety of peripherals as available in this format. Though the sockets support other devices, they are most often used to add wireless Ethernet cards from Broadcom, Foxconn (Atheros), or others.

The two MiniPCIe connects support PCIe and USB. One connector also alternatively supports an mSATA device in this socket. A sense circuit identifies the type of device present and auto-switches to handle either type.

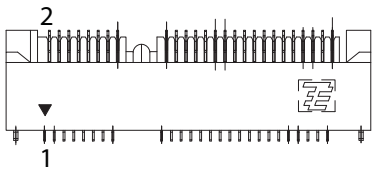
MC1 supports PCIe only.

MC2 supports either mSATA or PCIe. Use jumper “JPMSATA” on page 45 to select which device to use with MC2.

NOTE If JPMSATA is connected 1-2, MC2 is configured for PCIe operation and the pinout in the table below is correct.

When JPMSATA is connected 2-3, pins 23, 25, 31, and 33 change to SATA_RXp, SATA_RXn, SATA_TXn, SATA_TXp, respectively. This alternate pinout for CM2 is shown is parentheses.

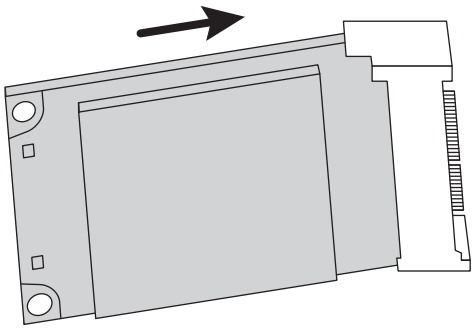
Layout and Pin Reference MC1 and MC2

Pin	Name	Pin	Name
			
1	WAKE#	2	3.3Vaux
3	COEX1	4	GND
5	COEX2	6	1.5V
7	CLKREQ#	8	UIM_PWR
9	GND	10	UIM_DATA
11	REFCLK-	12	UIM_CLK
13	REFCLK+	14	UIM_RESET
15	GND	16	UIM_VPP
Mechanical Key			
17	RSVD(UIM_C8)	18	GND
19	RSVD(UIM_C4)	20	W_DISABLE#
21	GND	22	PERST#
23	PERn0(SATA_RXp)	24	+3.3Vaux
25	PERp0(SATA_RXn)	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PETn0(SATA_TXn)	32	SMB_DATA
33	PETp0(SATA_TXp)	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3Vaux	40	GND
41	+3.3Vaux	42	LED_WWAN#
43	GND	44	LED_WLAN#
45	RSVD	46	LED_WPAN#
47	RSVD	48	+1.5V
49	RSVD	50	GND
51	RSVD	52	+3.3Vaux
Shaded cells indicate unconnected signals.			

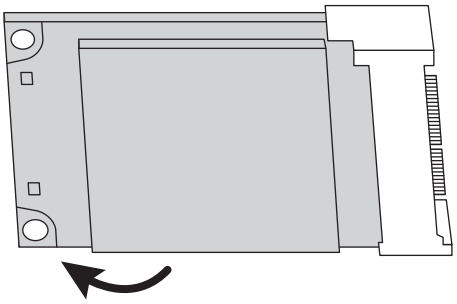
Additional Information

To install a miniPCIe/mSATA into MC1 or MC2:

1. Insert the miniPCIe/mSATA



2. Push the free end of the card toward the circuit board and then secure it with two (2 mm) screws (WinSystems P/N G527-0000-400).



Connector

Tyco 1775838-2 or equivalent

7.11 Jumpers

7.11.1 JPSATA SATA vs. CFast Selection

Select between SATA and CFast.

Layout and Pin Reference

	Jumper Positions	Selection
	JPSATA open	SATA only
	JPSATA Jumper 1-2	CFAST only
	JPSATA Jumper 2-3	Automatic detection of CFAST or SATA; CFAST will take precedence over SATA

7.11.2 JPMSATA

Select either MiniPCIe or mSATA at socket MC2.

Layout and Pin Reference

	Selection	Jumper Positions
	PCIe (L)	Jumper pins 1 and 2 together
	mSATA (H)	Jumper pins 2 and 3 together

7.11.3 JPLCDP Panel Power Jumper

Layout and Pin Reference

	Panel Power	Jumper Positions
	5V	Jumper pins 1 and 2 together (VGA)
	3.3V (Default)	Jumper pins 2 and 3 together (DP or LVDS)

Avoid simultaneous jumpering of pins 1-2 and 2-3. Mis-jumpering panel power causes damage to the board or the flat panel

Additional Information

The EPX-C414 has an integrated display controller that interfaces to both Analog VGA and flat panel displays. The video output mode is selected in the CMOS setup. Simultaneous flat panel and Analog VGA mode is also supported. The Analog VGA connector is located at VGA. WinSystems offers the cable CBL-VGA-002-12 to simplify the connection. The LVDS interface connector is located at **J7** to interface to flat panels. A backlight power connectors is located at BKLT. The panel power option selection is made at JPLCDP.

Contact a WinSystems Applications Engineer for information about available cable kits and supported panels.

This manual does not attempt to provide any information about how to connect to specific LCDs.

7.11.4 JPATX Power Supply Selection

Layout and Pin Reference

	Panel Power	Jumper Positions
	AT Power	Jumper pins 2 and 4 together When jumpered 2-4, the board powers up without pressing the power button.
	ATX Power	Jumper pins 4 and 6 together **With no battery installed:** When jumpered 4-6, the user must press the power button to power up the board. **With battery installed:** After the board has been powered and the power button pressed for the first time, the next action is controlled by the CMOS setting labeled “Power Loss Mode.” There are three options: • Keep last state • Always on • Always off

The EPX-C414 supports either AT (standard power supply) or ATX-type power supplies. WinSystems recommends using zero-load supplies. JPATX specifies the style of supply connected to the single board computer (SBC). An AT power supply is a simple on/off supply with no interaction with the single board computer. Most embedded systems use this type of power supply, and it is the default setting.

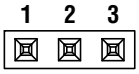
ATX-type power supplies function with a “soft” on/off power button and a +5VSB (standby). If an ATX compatible power supply is connected, set JPATX accordingly and connect a power button (momentary contact) between pin 3 (power button) and pin 2 (ground) of ATXAUX. The +5VSB signal provides the standby voltage to the EPX-C414 but does not power any other features of the board. When the power button is pressed, the EPX-C414 pulls PSON (Power Supply On) low and the power supply turns on all voltages to the single board computer. When the power button is pressed again, the BIOS signals the event so ACPI-compliant operating systems can be shutdown before the power is turned off. In ATX mode, if the power button is held for 4 seconds, the power supply is forced off, regardless of ACPI. Because this is software driven, it is possible that a software lockup could prevent the power button from functioning properly. For the BIOS to report the ATX supply to ACPI-compatible operating systems, JPATX must be setup correctly.

Pins 2-4-6 define what happens after G3 (all power removed) and when no battery is present.

7.11.5 JPDIO1 and JPDIO2 Digital I/O Power

The I/O connectors provide either +5V or +3.3V to an I/O rack for miscellaneous purposes through jumper configurations at JPDIO1 and JPDIO2. When JPDIO2 pins 2-3 are jumpered, +5V is provided at pin 49 of DIO1 and DIO2. If JPDIO2 pins 1-2 are jumpered, then +3.3V is provided at pin 49 of DIO1 and DIO2. Always ensure current is limited to a safe value (less than 400 mA) to avoid damaging the CPU board.

Layout and Pin Reference

	Jumper	LVDS setting
	1-2	+5V provided at pin 49 of DIO1/DIO2 (default)
	2-3	+3.3V provided at pin 49 of DIO1/DIO2
	Open	No power at pin 49 of DIO1/DIO2

7.11.6 JPBAT - Battery Enable

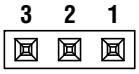
Enables or disables the battery.

To enable the battery, jump 2-1.

To disable the battery, jump 3-2 or remove the strap completely.

NOTE The battery must be installed at BAT before the battery can be enabled.

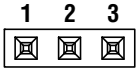
Layout and Pin Reference

	Jumper	RTC Battery Enable Setting
	1-2	Normal operation
	2-3	Resets time, date, and battery-backed RAM

7.11.7 JP5VSB - 5V Standby Power Select

Shorts 5V and 5V_SB. Connect pins 1-2 when using AT power supply; connect pins 2-3 or Open when using ATX power supply. Pin out as oriented: 1-2-3.

Layout and Pin Reference

	Jumper	5V Standby Power Setting
	1-2	Shorts +5V IN to +5V SB (default)
	2-3	+5V IN to N.C. (no connection)

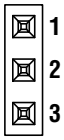
7.11.8 JP104P - PCI-104 Power Source Select

Configures power source for the PC/104-Plus (see “PC104P PC/104-Plus Bus” on page 41).

No power is supplied when jumped 1-2.

3.3V is supplied when jumped 2-3.

Layout and Pin Reference

	Jumper	PC/104-Plus Power Setting
	1-2	From Pin 5 of power connector (default)
	2-3	From onboard +3.3V

7.11.9 JPFPGA

JPFPGA is the JTAG programming header for the FPGA configuration EEPROM. JPFPGA is a 1x6 header reserved for manufacturer programming only.

7.11.10 JPMC1 and JPMC2 MiniPCie

The MiniPCie connectors at MC1 and MC2 include a jumper to disable the WLAN card, if installed. JPMC1 enables/disables WLAN at MC1. JPMC2 enables/disables WLAN at MC2.

Connector	Pin Reference
JPMC1	1-2 – Disables WLAN at MC1 2-3 – Enables WLAN at MC1
JPMC2	1-2 – Disables WLAN at MC2 2-3 – Enables WLAN at MC2

7.12 LED Indicators

7.12.1 LED1, LED2 Ethernet LEDs

There are two Ethernet controllers on the EPX-C414 board. On the top side of the board, two headers (LED1 and LED2) drive remotely mounted LEDs or other inputs. Each controller has three LEDs on the bottom of the board to indicate connectivity status. Refer to Table 21 for details.

Table 21: Ethernet LEDs

	Controller 1		Controller 2	
Function	Off Board Header	On Board LEDs	Off Board Header	On Board LEDs
Activity	LED1 pin 1	LED5	LED1 pin 1	LED8
Link 10	N/C	None	N/C	None
Link 100	LED1 pin 2	LED6	LED1 pin 2	LED9
Link 1000	LED1 pin 3	LED7	LED1 pin 3	LED10

Color indicates LED color.
Off board signals are active low.
Limit off board current to less than 20mA.
Activity LED is off when there is no LINK and flashes on data transfer.
Both yellow and red LEDs are off when link speed is 10Mbps.
Yellow LEDs are on when link speed is 100Mbps.
Red LEDs are on when link speed is 1000Mbps.
Channels are independent.

Layout and Pin Reference, top of board

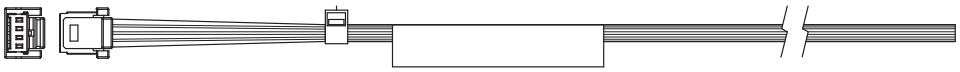
	Pin	Description
LED 1 (Ethernet Port 1) 1  4	1	Activity
	2	Speed 100
	3	Speed 1000
	4	+3.3V power
LED 2 (Ethernet Port 2) 1  4	1	Activity
	2	Speed 100
	3	Speed 1000
	4	+3.3 VSB power

Connectors

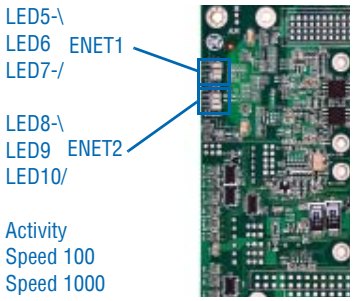
MOLEX 5019530407

Matching Connectors

- MOLEX 5019390400 (housing)
- MOLEX 501334-0100 or 501334-0000 (crimp)

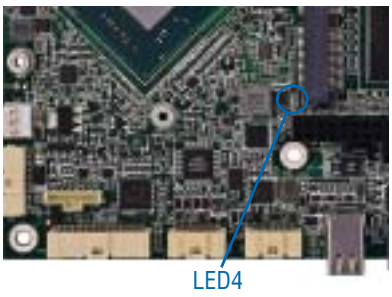


Layout and Reference, bottom of board

	Enet1	Enet2	Description
	LED5	LED8	Activity (green)
	LED6	LED9	Speed 100 (yellow)
	LED7	LED10	Speed 1000 (red)

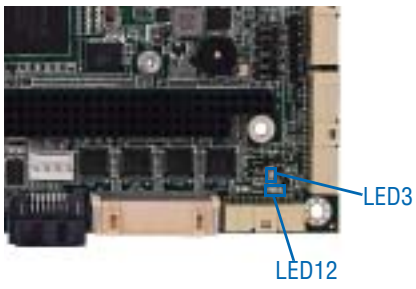
7.12.2 LED4 - Status LED

A status LED is populated on the board at LED4, to indicate activity. The LED is turned off during the boot process and can be turned on by writing 0x01 to hex address 0x29D. The status LED can then be toggled by writing 0x00 for off and 0x01 for on at the same address.



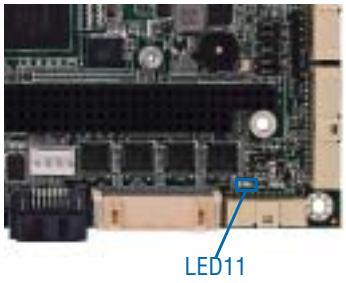
7.12.3 LED3 and 12 - Power LEDs

LED3 and LED12 are power indicators. (The LED3 reference designator is not visible on the board.) When no power is applied to the board, LED3 and LED12 are off. When power is applied but the board is in Standby, LED3 is yellow and LED12 is off. When the board is running, LED3 is off and LED12 is blue.



7.12.4 LED11 - SATA LED

LED11 indicates SATA activity. This LED flashes red during read or write operations.



8. BIOS

8.1 General Information

The EPX-C414 includes BIOS from Insyde® software to ensure full compatibility with PC operating systems and software. The basic system configuration is stored in battery-backed CMOS RAM within the clock/calendar. As an alternative, the CMOS configuration may be stored in EEPROM for operation without a battery. For more information of CMOS configuration, see the BIOS Settings Storage Options section of this manual. Access to this setup information is via the Setup Utility in the BIOS.

8.2 Entering Setup

To enter setup, power up the computer and press DEL when the splash screen is displayed. It may take a few seconds before the main setup menu screen is displayed.

8.3 Navigating the Menus

Use the Up and Down arrow keys to move among the selections and press Enter when a selection is highlighted to enter a sub-menu or to see a list of choices. Following are images of each menu screen in the default configuration along with a brief description of each option where applicable. Available options are listed in reference tables. Menu values shown in bold typeface are factory defaults.

8.4 BIOS Splash Screen

Custom BIOS Splash Screens can be accommodated for OEM customers. Please contact one of our Application Engineers for details.

Main Menu	
System Time	09:40:34
System Date	04/09/2010
>IDE Primary/Master	None
>IDE Primary/Slave	None
>SATA Port 1	None
>SATA Port 2	None
System Memory	633 KB
Extended Memory	2085888 KB
Ethernet MAC Address 1	xx:xx:xx:xx:xx:xx
Ethernet MAC Address 2	xx:xx:xx:xx:xx:xx
CPU Temperature	50°C/132°F
Ambient Temperature	40°C/104 °F

Each available option is listed in detail in the following sections. Navigation to the screens is located at the top of each screen's layout.

Depending on the Primary Master Type, various Primary Master options are available. See the following screens.

Main Menu > IDE Primary Master/Slave [None]	
Type	Auto
Multi-Sector Transfers	Disabled
LBA Mode Control	Disabled
32 Bit I/O	Disabled
Options	Disabled/Enabled
Transfer Mode	FPIO 4/DMA 2
Ultra DMA Mode	Disabled | (Mode 2 for IDE Primary Slave only)
SMART Monitoring	Disabled

Main Menu > SATA Port 1	
Type	Auto
Multi-Sector Transfers	Disabled
LBA Mode Control	Disabled
32 Bit I/O	Disabled
Options	Disabled/Enabled
Transfer Mode	Standard
Ultra DMA Mode	Disabled
SMART Monitoring	Disabled

Advanced	
Installed O/S	Win95
Options	Other/Win95/Win98 WinMe /Win2000
Reset Configuration Data	No
Options	
No Yes	
Large Disk Access Mode	DOS
Options	Other DOS
Summary screen	Disabled
Options	Disabled/Enabled
Boot-time Diagnostic Screen	Enabled
Options	Disabled/Enabled
QuickBoot Mode	Enabled
Options	Disabled/Enabled
Extended Memory Testing	None
Options	Normal /Just zero it/None

Intel
> CPU Control Sub-Menu
> Video (Intel IGD) Control Sub-Menu
> ICH Control Sub-Menu
> Super I/O Control Sub-Menu
> ACPI Control Sub-Menu

Intel > CPU Control Sub-Menu	
Hyperthreading	Enabled
Options	Disabled/Enabled
Processor Power Management	Enabled
Options	Disabled/GV3 Only
C-States Only Enabled	
Timestamp Counter Updates	Enabled
Options	Disabled/Enabled
> CPU Thermal Control Sub-Menu	
Set Max Ext CPUID = 3	Disabled
Options	Disabled/Enabled

Intel > CPU Control Sub-Menu > CPU Thermal Control Sub-Menu	
Thermal Control Circuit	Disabled
Options	Disabled/TM1
DTS Enable	Disabled
Options	Disabled/Enabled
Active Trip Point	55 C
Options	Disabled/55 C
63 C	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
Passive Cooling Trip Point	95 C
Options	Disabled/55 C
63 C	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
Passive TC1 Value	1
Passive TC2 Value	5
Options	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
Passive TSP Value	10
Options	
10	
20	
30	

Intel > CPU Control Sub-Menu > CPU Thermal Control Sub-Menu	
40	
50	
60	
70	
80	
90	
100	
110	
120	
130	
140	
150	
Critical Trip Point	POR
Options	
POR 15 C	
23 C	
31 C	
39 C	
47 C	
55 C	
63 C	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
127 C	

Intel > Video (Intel IGD) Control Sub-Menu	
IGD - VBIOS Boot Type	CRT
Options	VBT/Default/CRT
LFP CRT+LFP	
> IGD - LCD Control Sub-Menu	
DVMT 4.0 Mode	Auto
Options	Fixed/DVMT
Auto	

Intel > Video (Intel IGD) Control Sub-Menu > IGD - LCD Control Sub-Menu	
IGD - LCD Panel Type	3: 1024x768 LVDS
Options:	
1: 640x480	LVDS
2: 800x600	LVDS
3: 1024x768	LVDS
4: 1024x600	LVDS
5: 800x480	LVDS
6: Reserved	
7: Reserved	
8: 1280x768 LVDS	
9: Reserved	
10: Reserved	
11: Reserved	
12: Reserved	
13: Reserved	
14: 1280X800 LVDS	
15: 1280X600 LVDS	
16: Reserved	
IGD - Panel Scaling	Auto
Options	
Auto	
Force Scaling Off	
GMCH BLC Control	GMBus
Options	Disabled/PWM
GMBus	
BIA Control	Disabled
Options	Automatic/Disabled/ Level 1
Level 2	
Level 3	
Level 4	
Level 5	
Spread Spectrum Clock Chip	Off
Options	Off/Hardware/ Software

Intel > ICH Control Sub-Menu	
> Integrated Device Control Sub-Menu	
Pop Up Mode Enable	Enabled
Options	Disabled/Enabled
Pop Down Mode Enable	Enabled
Options	Disabled/Enabled
LPC Decode Range 1 Base Address	300h
LPC Decode Range 1 Size	64 Bytes
Options	
64 Bytes	
32 Bytes	
16 Bytes	
8 Bytes	
4 Bytes	
LPC Decode Range 2 Base Address	500h
LPC Decode Range 2 Size	256 Bytes
Options	
256 Bytes	
128 Bytes	
64 Bytes	
32 Bytes	
16 Bytes	
8 Bytes	
4 Bytes	

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu	
> PCI Express Control Sub-Menu	
> ICH USB Control Sub-Menu	
Azalia HD Audio Function	Auto
Options	Disabled/Auto
SATA/PATA Configuration	Enhanced
Options	Compatible/ Enhanced
AHCI Configuration	Disabled
Options	Disabled/Enabled
Disable Vacant Ports	Disabled
Options	Disabled/Enabled
On-board LAN	Enabled
Options	Disabled/Enabled
PXE OPROM	Disabled

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > PCI Express Control Sub-Menu	
PCI Express - Root Port 1	Enabled
Options	Disabled/Enabled/ Auto
PCI Express - Root Port 2	Auto
Options	Disabled/Enabled/ Auto
Root Port ASPM Support	Auto
Options	Disabled/Auto
ASPM Latency Checking	Auto
Options	Disabled/Auto
> PCI/PNP ISA IRQ Resource Exclusion	

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > PCI Express Control Sub-Menu PCI/PNP ISA IRQResource Exclusion	
IRQ 3	Available
Options	Available/Reserved
IRQ 4	Available
Options	Available/Reserved
IRQ 5	Available
Options	Available/Reserved
IRQ 7	Available
Options	Available/Reserved
IRQ 9	Available
Options	Available/Reserved
IRQ 10	Reserved
Options	Available/Reserved
IRQ 11	Available
Options	Available/Reserved

Intel > ICH Control Sub-Menu > Integrated Device Control Sub-Menu > ICH USB Control Sub-Menu	
Overcurrent Detection	Enabled
Options	Disabled/Enabled

Intel > Super I/O Control Sub-Menu	
Serial port 1	Enabled
Speed	Low
Base I/O address	3F8
Interrupt	IRQ 4
Interface	RS232
Options	
Port x	
Speed	Disabled/Enabled
Base I/O address	Low/High
3F8	
2F8	
3E8	
2E8	Interrupt
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	
IRQ 9	Interface
RS232 RS422 RTS	
RS422 Auto RS485 RTS	
RS485 RTS w/Echo RS485 Auto	
RS485 Auto w/Echo	
Serial port 2	Enabled
Speed	Low
Base I/O address	2F8
Interrupt	IRQ 3
Interface	RS232
Options	
Port x	
Speed	Disabled/Enabled
Base I/O address	Low/High
3F8	
2F8	
3E8	
2E8	Interrupt
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	
IRQ 9	Interface
RS232 RS422 RTS	
RS422 Auto RS485 RTS	
RS485 RTS w/Echo RS485 Auto	
RS485 Auto w/Echo	
Serial port 3	Enabled
Speed	Low

Intel > Super I/O Control Sub-Menu	
Base I/O address	3E8
Interrupt	IRQ 5
Interface	RS232
Options	
Port x	
Speed	Disabled/Enabled
Base I/O address	Low/High
3F8	
2F8	
3E8	
2E8	Interrupt
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	Interface
RS232 RS422 RTS	
RS422 Auto RS485 RTS	
RS485 RTS w/Echo RS485 Auto	
RS485 Auto w/Echo	
Serial port 4	Enabled
Speed	Low
Base I/O address	2E8
Interrupt	IRQ 6
Interface	RS232
Options	
Port x	
Speed	Disabled/Enabled
Base I/O address	Low/High
3F8	
2F8	
3E8	
2E8	Interrupt
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	Interface
RS232 RS422 RTS	
RS422 Auto RS485 RTS	
RS485 RTS w/Echo RS485 Auto	
RS485 Auto w/Echo	
Parallel port	Enabled
Base I/O address	378
Interrupt	IRQ 7
Options	
Port x	
Disabled Enabled	Base I/O address

Intel > Super I/O Control Sub-Menu	
378	
278	Interrupt
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	
IRQ 9	
IRQ 10	
IRQ 12	
Digital I/O port	Enabled
DIO port address	120
DIO IRQ	IRQ 10
Options	
Digital I/O port	
Disabled Enabled	DIO port address
120	
130	
140	DIO IRQ
Disabled IRQ 3	
IRQ 4	
IRQ 5	
IRQ 6	
IRQ 7	
IRQ 9	
IRQ 10	
IRQ 12	
Watchdog	0
Options	
{Enter any value between 0-255 for seconds.}	
SIO Firmware	Rev 0006

Intel > ACPI Control Sub-Menu	
Active Trip Point	55 C
Options	Disabled/55 C
63 C	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
Passive Cooling Trip Point	95 C
Options	Disabled/55 C
63 C	

Intel > ACPI Control Sub-Menu	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
Passive TC1 Value	1
Passive TC2 Value	5
Options	
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
Passive TSP Value	10
Options	
10	
20	
30	
40	
50	
60	
70	
80	
90	
100	
110	
120	
130	
140	
150	
Intel > ACPI Control Sub-Menu (continued)	
Critical Trip Point	POR
Options	
POR 15 C	

Intel > ACPI Control Sub-Menu	
23 C	
31 C	
39 C	
47 C	
55 C	
63 C	
71 C	
79 C	
87 C	
95 C	
103 C	
111 C	
119 C	
127 C	
FACP - RTC S4 Flag Value	Enabled
Options	Disabled/Enabled
FACP - PM Timer Flag Value	Enabled
Options	Disabled/Enabled
HPET Support:	Disabled
Options	Disabled/Enabled

Security	
Supervisor Password Is	Clear
User Password Is	Clear
Set Supervisor Password	Enter
Set User Password	Enter
Virus check reminder	Disabled
Options	Disabled/Daily/Weekly/Monthly
Password on boot	Disabled

Boot
Boot priority order
1
2
3
4
5
6
7
8
Options
Excluded from boot order
Options
All IDE HDD
All USB Floppy All USB KEY All USB HDD
All USB CDROM All USB ZIP
All USB LS120 All PCI BEV
Bootable Add-in Cards

Exit
Exit Saving Changes
Exit Saving Changes to CMOS and EEPROM
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes

8.5 BIOS Setting Storage Options

The EPX-C414 includes BIOS from Insyde software to ensure full compatibility with PC operating systems and software. The basic system configuration is stored in non-volatile memory.

Access to this setup information is via the Setup Utility in the BIOS.

9. Cables

WinSystems cables and batteries simplify connection to the EPX-C414. The following table lists available items.

Table 22: Cable and Battery Specifications

Item	Part Number	Connection	Description
Cables	CBL-265-G-2-1.5	See “PWR Power and Reset” on page 21	Power connection
	CBL-USB4-002-12	See “USB1, USB2 - USB 2.0 Ports” on page 33	USB - dual 2 mm Molex Milli-Grid, 12”
	ADP-IO-USB-001		
	CBL-VGA-002-12	See “VGA Analog VGA Connector” on page 26	
	CBL-AUDIO7-102-12	See “AUDIO HD Audio Connector” on page 29	Full 7.1 audio support.
	CBL-AUDIO2-102-12		Basic Line In, Line Out, and microphone audio support
	CBL-AUDIO5-102-12		5.1 Audio support
	CBL-ENET2-002-12	See “LAN Ethernet Port” on page 36	Ethernet 2x10, 1.25 mm to 2 x RJ-45 female/jack 12” dual 12 pin,2 mm to dual RJ-45
	ADP-IO-ENET-001		Dual 12 pin,2 mm to dual RJ-45
	CBL-BKLT-000-14	See “BKLT Backlight Power Connector” on page 28	Backlight 1x11 1 mm, unterminated Pico-clasp
	CBL-DIO24-001-12	See “DIO1, DIO2 Digital Input/ Output” on page 37	DIO 2x25 1 mm to 2x25 1 mm, 12”
	CBL-DIO24-002-12		DIO cable 2x25 1 mm to 2x25 .1 CNTRS 12”
	CBL-LPT-002-12	See “LPT Parallel Printer Port Connector” on page 25	LPT cable 2x15, 1 mm, to DB25 12”
	CBL-LVDS24-000-134	See “LVDS Connector” on page 27	LVDS 2x20, 1 mm to unterminated 14”
Batteries	BAT-LTC-E-36-16-2	See “BAT External Battery Connector” on page 23	External 3.6V, 1650 mAH battery with plug-in connector
	BAT-LTC-E-36-27-2		External 3.6V, 2700 mAH battery with plug-in connector

10. Software Drivers

Go to www.winsystems.com for information on available software drivers.

Appendix A. Best Practices

The following paragraphs outline the best practices for operating the EPX-C414 in a safe, effective manner, that does not damage the board. Please read this section carefully.

Power Supply

Avoid Electrostatic Discharge (ESD)—Only handle the circuit board and other bare electronics when electrostatic discharge (ESD) protection is in place. Having a wrist strap and a fully grounded workstation is the minimum ESD protection required before the ESD seal on the product bag is broken.

Power Supply Budget

Evaluate your power supply budget. It is usually good practice to budget twice the typical power requirement for all of your devices.

Zero-load Power Supply

Use a zero-load power supply whenever possible. A zero-load power supply does not require a minimum power load to regulate. If a zero-load power supply is not appropriate for your application, then verify that the single board computer's typical load is not lower than the power supply's minimum load. If the single board computer does not draw enough power to meet the power supply's minimum load, then the power supply does not regulate properly and can cause damage to the EPX-C414.

Use Proper Power Connections (Voltage)—When verifying the voltage, measure it at the power connector on the EPX-C414. Measuring it at the power supply does not account for voltage drop through the wire and connectors.

The EPX-C414 requires +5V (±5%) to operate. Verify the power connections. Incorrect voltages can cause catastrophic damage.

Populate all of the +5V and ground connections. Most single board computers have multiple power and ground pins, and all of them should be populated. The more copper connecting the power supply to the EPX-C414, the better.

Adjusting Voltage

If you have a power supply that allows you to adjust the voltage, it is a good idea to set the voltage at the power connector of the EPX-C414 to 5.1V. The EPX-C414 can tolerate up to 5.25V, so setting your power supply to provide 5.1V is safe and allows for the small amount of voltage drop that occurs over time as the power supply ages and the connector contacts oxidize.

Power Harness

Minimize the length of the power harness. This reduces the amount of voltage drop between the power supply and the EPX-C414.

Gauge Wire

Use the largest gauge wire that you can. Most connector manufacturers have a maximum gauge wire they recommend for their pins. Try going one size larger; it usually works and the extra copper helps your system perform properly over time.

Contact Points

WinSystems' boards mostly use connectors with gold finish contacts. Gold finish contacts are used exclusively on high-speed connections. Power and lower speed peripheral connectors may use a tin finish as an alternative contact surface. It is critical that the contact material in the mating connectors is matched properly (gold to gold and tin to tin). Contact areas made with dissimilar metals can cause oxidation/corrosion, resulting in unreliable connections.

Pin Contacts

Often the pin contacts used in cabling are not given enough attention. The ideal choice for a pin contact would include a design similar to Molex's or Trifurcon's designs, which provide three distinct points to maximize the contact area and improve connection integrity in high shock and vibration applications.

Power Down

Make sure that power has been removed from the system before making or breaking any connections.

Power Supply OFF—The power supply should always be off before it is connected to the I/O Module. Do not hot-plug the EPX-C414 on a host platform that is already powered.

I/O Connections OFF—I/O Connections should also be off before connecting them to the embedded computer modules or any I/O cards. Connecting hot signals can cause damage whether the embedded system is powered or not.

Mounting and Protecting the I/O Module

The EPX-C414 must be mounted properly to avoid damage. Standoff kits are available and recommended for use with the EPX-C414.

- KIT-PCM-STANDOFF-4: Four piece nylon hex PC/104 standoff kit
- KIT-PCM-STANDOFF-B-4: Four piece brass hex PC/104 standoff kit

The following table lists the items contained in each kit.

Table 22: Standoff kits

Kit	Component	Description	Qty
KIT-PCM-STANDOFF-4 4 pc. nylon hex PC/104 standoff kit	Standoff	Nylon 0.25” hex, 0.600” long male/female 4-40	4
	Hex nut	Hex nylon 4-40	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4
KIT-PCM-STANDOFF-B-4 4 pc. brass hex PC/104 standoff kit	Standoff	Brass 5 mm hex, 0.600” long male/female 4-40	4
	Hex nut	4-40 x 0.095 thick, nickel finish	4
	Screw	Phillips-pan head (PPH) 4-40 x 1/4” stainless steel	4

Placing the EPX-C414 on Mounting Standoffs—Be careful when placing the EPX-C414 on the mounting standoffs. Sliding the board around until the standoffs are visible from the top can cause component damage on the bottom of the board.

Do Not Bend or Flex the EPX-C414—Bending or flexing can cause irreparable damage. Embedded computer modules are especially sensitive to flexing or bending around Ball Grid Array (BGA) devices. BGA devices are extremely rigid by design and flexing or bending the embedded computer module can cause the BGA to tear away from the printed circuit board.

Mounting Holes—The mounting holes are plated on the top, bottom and through the barrel of the hole and are connected to the embedded computer module’s ground plane. Traces are often routed in the inner layers right below, above or around the mounting holes.

- Never use a drill or any other tool in an attempt to make the holes larger.
- Never use screws with oversized heads. The head could come in contact with nearby components causing a short or physical damage.
- Never use self-tapping screws; they compromise the walls of the mounting hole.
- Never use oversized screws that cut into the walls of the mounting holes.
- Always use all of the mounting holes. By using all of the mounting holes, you provide the support the embedded computer module needs to prevent bending or flexing.

Plug or Unplug Connectors Only on Fully Mounted Boards—Never plug or unplug connectors on a board that is not fully mounted. Many of the connectors fit rather tightly and the force needed to plug or unplug them could cause the embedded computer module to be flexed.

Avoid Cutting the EPX-C414—Never use star washers or any fastening hardware that cut into the EPX-C414.

Avoid Over-tightening of Mounting Hardware—Causing the area around the mounting holes to compress could damage interlayer traces around the mounting holes.

Use Appropriate Tools—Always use tools that are appropriate for working with small hardware. Large tools can damage components around the mounting holes.

Avoid Conductive Surfaces—Never allow the embedded computer module to be placed on a conductive surface. Many embedded systems use a battery to back up the clock-calendar and CMOS memory. A conductive surface such as a metal bench can short the battery causing premature failure.

Adding PC/104 Boards to Your Stack

Be careful when adding PC/104 boards to your stack—Never allow the power to be turned on when a PC/104 board has been improperly plugged onto the stack. It is possible to misalign the PC/104 card and leave a row of pins on the end or down the long side hanging out of the connector. If power is applied with these pins misaligned, it causes the I/O board to be damaged beyond repair.

Conformal Coating

Conformal coating by any source other than WINSYSTEMS voids the product warranty and will not be accepted for repair by WINSYSTEMS. If such a product is sent to WINSYSTEMS for repair, it will be returned at customer expense and no service will be performed. A WINSYSTEMS product conformally coated by WINSYSTEMS will be subject to regular WINSYSTEMS warranty terms and conditions.

Operations/Product Manuals

Every single board computer has an Operations manual or Product manual.

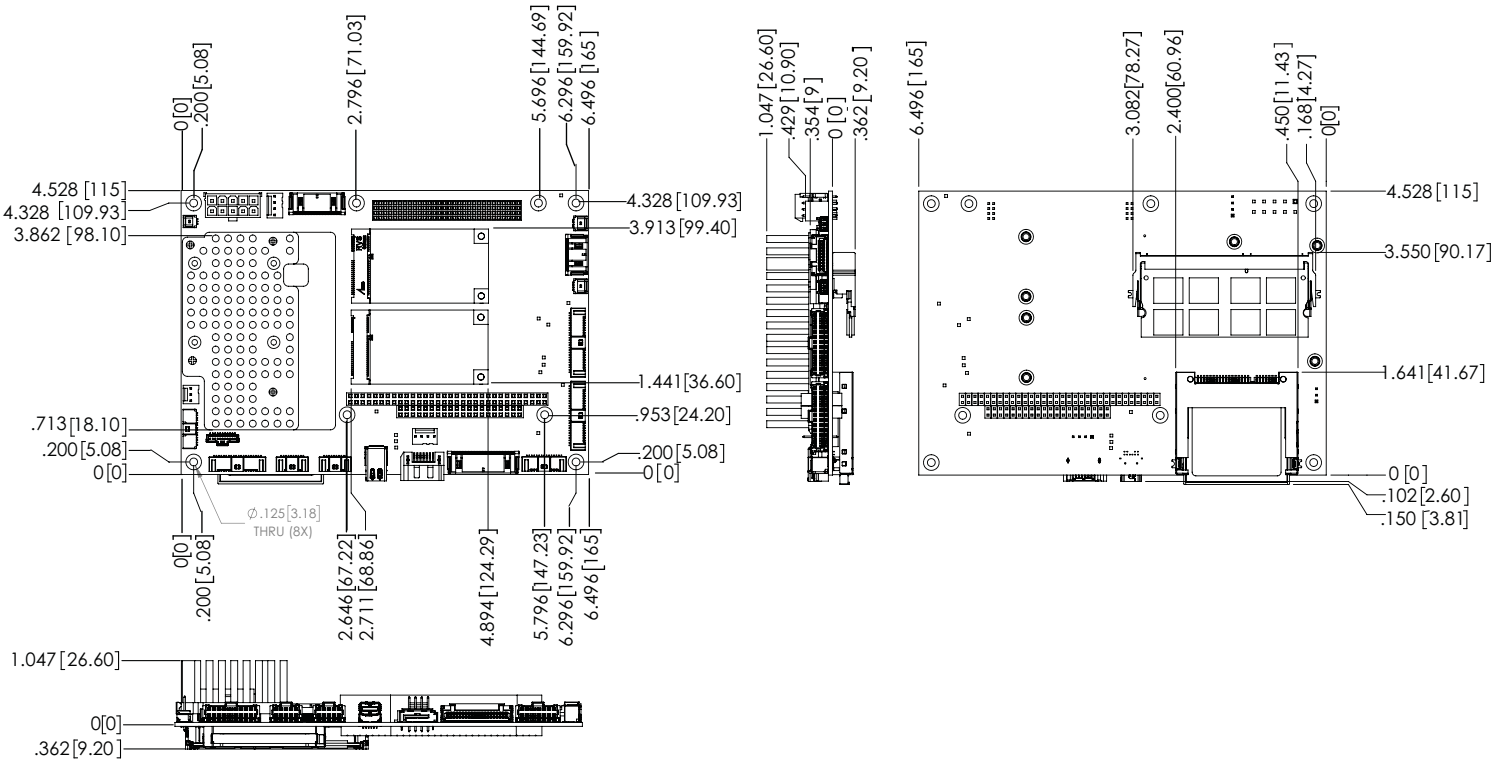
Periodic Updates—Operations/Product manuals are updated often. Periodically check the WinSystems website (https://www.winsystems.com) for revisions.

Check Pinouts—Always check the pinout and connector locations in the manual before plugging in a cable. Many I/O modules have identical headers for different functions and plugging a cable into the wrong header can have disastrous results.

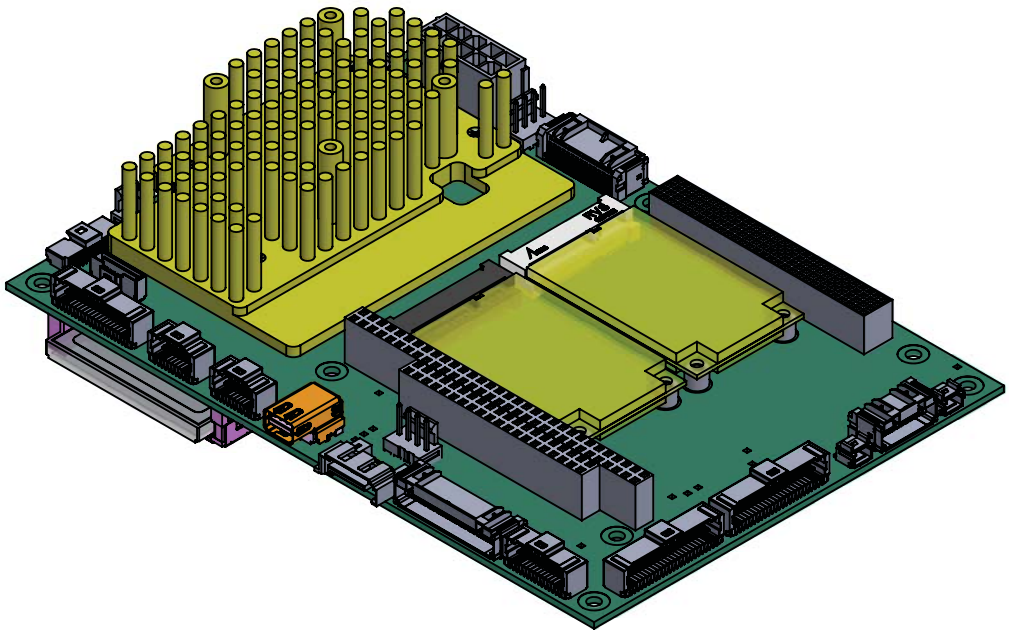
Contact an Applications Engineer—If a diagram or chart in a manual does not seem to match your board, or if you have additional questions, contact a WinSystems Applications Engineer at: +1-817-274-7553.

Appendix B. Mechanical Drawings

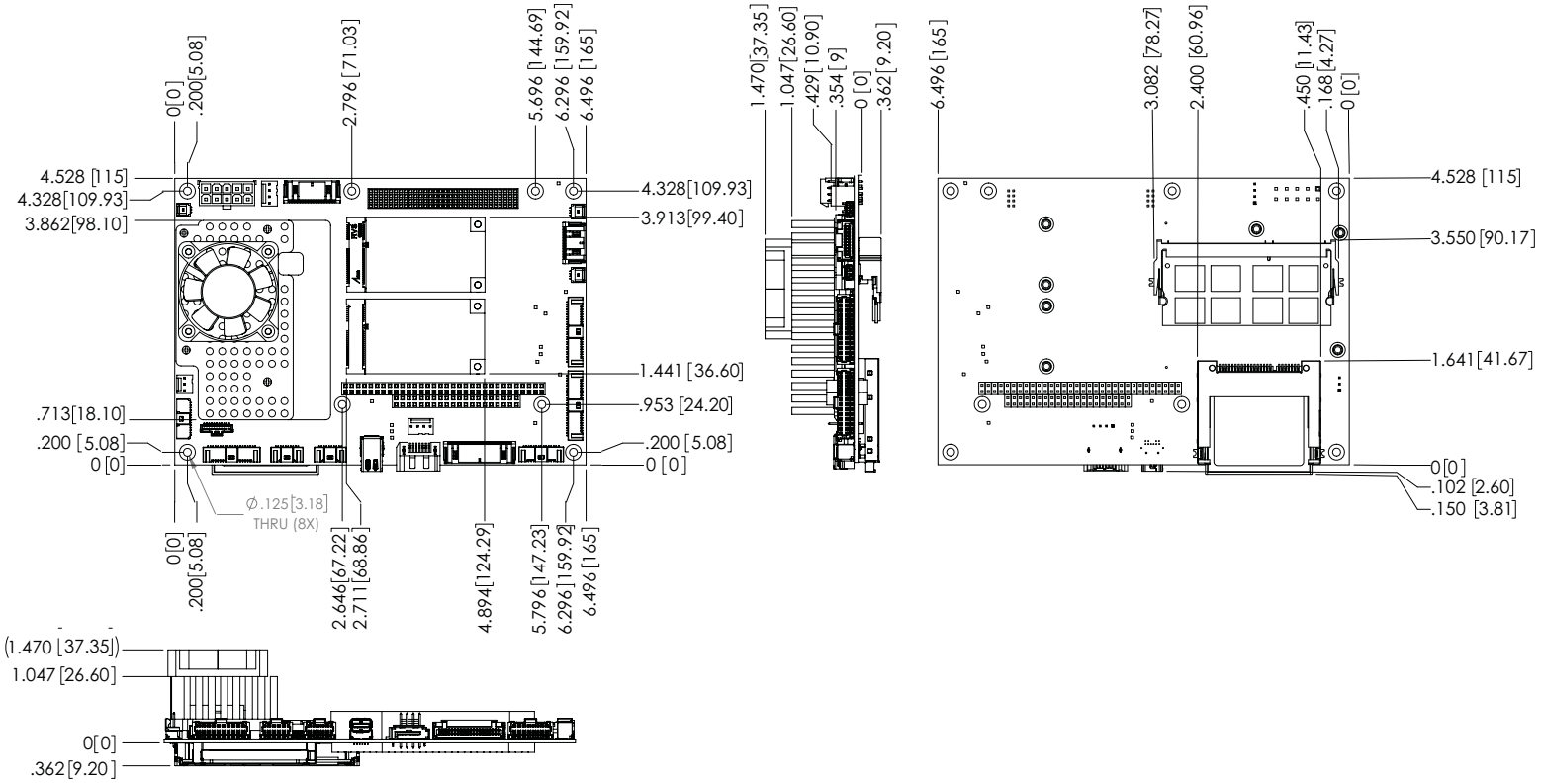
EPX-C414 Dual-core, no fan (Layout 2d)



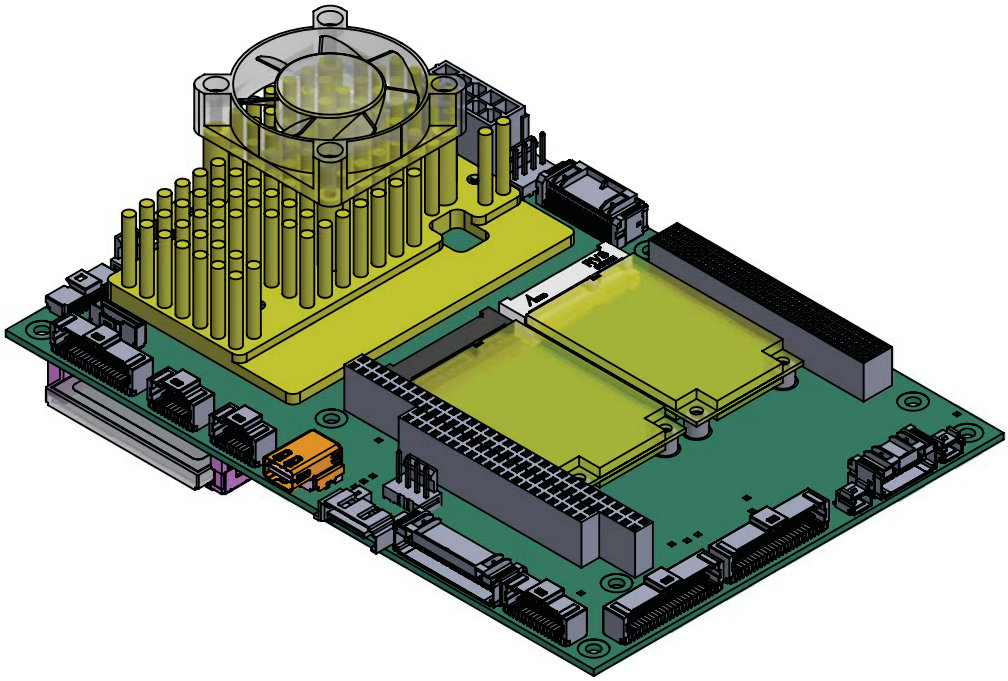
UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES [MILLIMETER]
BOARD IS SHOWN WITH OPTIONAL CFAST, MEMORY, AND DUAL MINI-PCIe.



EPX-C414 Quad-core, with fan (Layout 1q)



UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES [MILLIMETER]
BOARD IS SHOWN WITH OPTIONAL CPU's FAN, CFAST, MEMORY, AND DUAL MINI-PCIe.



Appendix C. Power-on Self-Test (POST) Codes

If the system hangs before the BIOS can process the error, the value displayed at the I/O port address 80h is the code of the last successful operation. In this case, the screen does not display an error code.

POST_CODE()

Use the POST_CODE() macro to output a number (Data) to the configured I/O port or status code.

Prototype

```
#include "InsydeModulePkg/Include/PostCode.h" POST_CODE(Data)
```

Parameters

Data: Unsigned integer that specifies the POST Code value. Must be between 0x00 and 0xff.

POST Codes

POST Codes are 8-bit unsigned integer values that are sent to a specific I/O port (where hardware can decode and display the value) or to the DDT debugger.

8-Bit POST Code Ranges

This table shows the overview of the 8-Bit POST Code Ranges used by InsydeH2O.

Table 23: 8-Bit POST Code Ranges

Phase	POST Code Value Ranges
SEC	0x01 - 0x0F
PEI	0x70 - 0x9F
DXE	0x40 - 0x6F
BDS	0x10 - 0x3F
SMM	0xA0 - 0xBF
S3	0xC0 - 0xCF
ASL	0x51 - 0x55
	0xE1 - 0xE4
PostBDS	0xF9 - 0xFE
Insyde H2ODDT Reserved	0xD0 - 0xD7
OEM Reserved	0xE8 - 0xEB
Reserved	0xD8 - 0xE0
	0xE5 - 0xE7
	0xEC - 0xF8

SEC Phase

Table 24: SEC Phase 8-Bit POST Code Values

Value	Functionality Name	Description
01	SEC_SYSTEM_POWER_ON CPU	Power on and switch to Protected mode
02	SEC_BEFORE_MICROCODE_PATCH	Patching CPU microcode
03	SEC_AFTER_MICROCODE_PATCH	Setup Cache as RAM
04	SEC_ACCESS_CSR PCIE MMIO	Base Address initial
05	SEC_GENERIC_MSRINIT CPU	Generic MSR initialization
06	SEC_CPU_SPEEDCFG	Setup CPU speed
07	SEC_SETUP_CAR_OK	Cache as RAM test
08	SEC_FORCE_MAX_RATIO	Tune CPU frequency ratio to maximum level
09	SEC_GO_TO_SECSTARTUP	Setup BIOS ROM cache
0A	SEC_GO_TO_PEICORE	Enter Boot Firmware Volume

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

PEI Phase

Table 25: PEI Phase 8-Bit POST Code Values

Value	Functionality Name	Description
70	PEI_SIO_INIT	Super I/O initialization
71	PEI_CPU_REG_INIT	CPU Early Initialization
72	PEI_CPU_AP_INIT	Multi-processor Early initialization
73	PEI_CPU_HT_RESET	HyperTransport initialization
74	PEI_PCIE_MMIO_INIT	PCIE MMIO BAR Initialization
75	PEI_NB_REG_INIT	North Bridge Early Initialization
76	PEI_SB_REG_INIT	South Bridge Early Initialization
77	PEI_PCIE_TRAINING	PCIE Training
78	PEI_TPM_INIT	TPM Initialization
79	PEI_SMBUS_INIT	SMBUS Early Initialization
7A	PEI_PROGRAM_CLOCK_GEN	Clock Generator Initialization
7B	PEI_IGD_EARLY_INITIAL	Internal Graphic device early initialization
7C	PEI_HECI_INIT	HECI Initialization
7D	PEI_WATCHDOG_INIT	Watchdog timer initialization
7E	PEI_MEMORY_INIT	Memory Initialization for Normal boot.
7F	PEI_MEMORY_INIT_FOR_CRISIS	Memory Initialization for Crisis Recovery
80	PEI_MEMORY_INSTALL	Simple Memory test
81	PEI_TXTPEI TXT	Function early initialization
82	PEI_SWITCH_STACK	Start to use Memory
83	PEI_MEMORY_CALLBACK	Set cache for physical memory

Value	Functionality Name	Description
84	PEI_ENTER_RECOVERY_MODE	Recovery device initialization
85	PEI_RECOVERY_MEDIA_FOUND	Found Recovery image
86	PEI_RECOVERY_MEDIA_NOT_FOUND	Recovery image not found
87	PEI_RECOVERY_LOAD_FILE_DONE	Load Recovery Image complete
88	PEI_RECOVERY_START_FLASH	Start Flash BIOS with Recovery image
89	PEI_ENTER_DXEIPL	Loading BIOS image to RAM
8A	PEI_FINDING_DXE_CORE	Loading DXE core
8B	PEI_GO_TO_DXE_CORE	Enter DXE core
8C	PEI_IFFS_TRANSITION_START	iFFS Transition Start
8D	PEI_IFFS_TRANSITION_END	iFFS Transition End

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

DXE Phase

Table 26: DXE Phase 8-Bit POST Code Values

Value	Functionality Name	Description
40	DXE_TCGDXE	TPM initialization in DXE
41	DXE_SB_SPI_INIT	South bridge SPI initialization
42	DXE_CF9_RESET	Setup Reset service
43	DXE_SB_SERIAL_GPIO_INIT	South bridge Serial GPIO initialization
44	DXE_SMMACCESS	Setup SMM ACCESS service
45	DXE_NB_INIT	North bridge Middle initialization
46	DXE_SIO_INIT	Super I/O DXE initialization
47	DXE_LEGACY_REGION	Set up Legacy Region service
48	DXE_SB_INIT	South Bridge Middle Initialization
49	DXE_IDENTIFY_FLASH_DEVICE	Identify Flash device
4A	DXE_FTW_INIT	Fault Tolerant Write verification
4B	DXE_VARIABLE_INIT	Variable Service Initialization
4C	DXE_VARIABLE_INIT_FAIL	Fail to initialize Variable Services
4D	DXE_MTC_INIT	MTC Initialization
4E	DXE_CPU_INIT	CPU middle-phase initialization
4F	DXE_MP_CPU_INIT	Multi-processor middle-phase initialization
50	DXE_SMBUS_INIT	SMBUS Initialization
51	DXE_SMART_TIMER_INIT	8259 Initialization
52	DXE_PCRTC_INIT	RTC Initialization
53	DXE_SATA_INIT	SATA Controller early initialization
54	DXE_SMM_CONTROLER_INIT	Setup SMM Control service
55	DXE_LEGACY_INTERRUPT	Setup legacy interrupt services
56	DXE_RELOCATE_SMBASE	Relocate SMM BASE
57	DXE_FIRST_SMI	SMI test
58	DXE_VTD_INIT	VTD Initialization

Value	Functionality Name	Description
59	DXE_BEFORE_CSM16_INIT	Legacy BIOS initialization
5A	DXE_AFTER_CSM16_INIT	Legacy interrupt function initialization
5B	DXE_LOAD_ACPI_TABLE	ACPI Table Initialization
5C	DXE_SB_DISPATCH	Setup SB SMM Dispatcher service
5D	DXE_SB_IOTRAP_INIT	Setup SB IOTRAP Service
5E	DXE_SUBCLASS_DRIVER	Build AMT Table
5F	DXE_PPM_INIT	PPM Initialization
60	DXE_HECIDRV_INIT	HECIDRV Initialization
61	DXE_VARIABLE_RECLAIM	Variable store garbage collection and reclaim operation
62	DXE_FLASH_PART_NONSUPPORT	Flash part not supported

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

BDS Phase

Table 27: BDS Phase 8-Bit POST Code Values

Value	Functionality Name	Description
10	BDS_ENTER_BDS	Enter BDS entry
11	BDS_INSTALL_HOTKEY	Install Hotkey service
12	BDS_ASF_INIT	ASF Initialization
13	BDS_PCI_ENUMERATION_START	PCI enumeration
14	BDS_BEFORE_PCIIO_INSTALL	PCI resource assign complete
15	BDS_PCI_ENUMERATION_END	PCI enumeration complete
16	BDS_CONNECT_CONSOLE_IN	Keyboard Controller, Keyboard and Mouse initialization
17	BDS_CONNECT_CONSOLE_OUT	Video device initialization
18	BDS_CONNECT_STD_ERR	Error report device initialization
19	BDS_CONNECT_USB_HC	USB host controller initialization
1A	BDS_CONNECT_USB_BUS	USB BUS driver initialization
1B	BDS_CONNECT_USB_DEVICE	USB device driver initialization
1C	BDS_NO_CONSOLE_ACTION	Console device initialization fail
1D	BDS_DISPLAY_LOGO_SYSTEM_INFO	Display logo or system information
1E	BDS_START_IDE_CONTROLLER	IDE controller initialization
1F	BDS_START_SATA_CONTROLLER	SATA controller initialization
20	BDS_START_ISA_ACPI_CONTROLLER	SIO controller initialization
21	BDS_START_ISA_BUS	ISA BUS driver initialization
22	BDS_START_ISA_FDD	Floppy device initialization
23	BDS_START_ISA_SEIRAL	Serial device initialization
24	BDS_START_IDE_BUS	IDE device initialization
25	BDS_START_AHCI_BUS	AHCI device initialization
26	BDS_CONNECT_LEGACY_ROM	Dispatch option ROMs
27	BDS_ENUMERATE_ALL_BOOT_OPTION	Get boot device information
28	BDS_END_OF_BOOT_SELECTION	End of boot selection
29	BDS_ENTER_SETUP	Enter Setup Menu
2A	BDS_ENTER_BOOT_MANAGER	Enter Boot manager
2B	BDS_BOOT_DEVICE_SELECT	Try to boot system to OS

Value	Functionality Name	Description
2C	BDS_EFI64_SHADOW_ALL_LEGACY_ROM	Shadow Misc Option ROM
2D	BDS_ACPI_S3SAVE	Save S3 resume required data in RAM
2E	BDS_READY_TO_BOOT_EVENT	Last Chipset initialization before boot to OS
2F	BDS_GO_LEGACY_BOOT	Start to boot Legacy OS
30	BDS_GO_UEFI_BOOT	Start to boot UEFI OS
31	BDS_LEGACY16_PREPARE_TO_BOOT	Prepare to Boot to Legacy OS
32	BDS_EXIT_BOOT_SERVICES	Send END of POST Message to ME via HECI
33	BDS_LEGACY_BOOT_EVENT	Last chipset initialization before boot to Legacy OS.
34	BDS_ENTER_LEGACY_16_BOOT	Ready to Boot Legacy OS.
35	BDS_RECOVERY_START_FLASH	Fast recovery start flash
36	BDS_START_SDHC_BUS SDHC	device initialization
37	BDS_CONNECT_ATA_LEGACY ATA	legacy device initialization
38	BDS_CONNEC_SD_LEGACY SD	legacy device initialization

NOTE The shaded rows in the table indicate the related functions are not from InsydeH2O (platform dependent).

PostBDS Phase

Table 28: BDS Phase 8-Bit POST Code Values

Value	Functionality Name	Description
F9	POST_BDS_NO_BOOT_DEVICE	No Boot Device
FB	POST_BDS_START_IMAGE	UEFI Boot Start Image
FD	POST_BDS_ENTER_INT19	Legacy 16 boot entry
FE	POST_BDS_JUMP_BOOT_SECTOR	Try to Boot with INT 19

S3

Table 29: S3 8-Bit POST Code Values

Value	Functionality Name	Description
C0	S3_RESTORE_MEMORY_CONTROLLER	Memory initialization for S3 resume
C1	S3_INSTALL_S3_MEMORY	Get S3 resume required data from memory
C2	S3_SWITCH_STACK	Start to use memory during S3 resume
C3	S3_MEMORY_CALLBACK	Set cache for physical memory during S3 resume
C4	S3_ENTER_S3_RESUME_PEIM	Start to restore system configuration
C5	S3_BEFORE_ACPI_BOOT_SCRIPT	Restore system configuration stage 1
C6	S3_BEFORE_RUNTIME_BOOT_SCRIPT	Restore system configuration stage 2
C7	S3_BEFORE_RELOCATE_SMM_BASE	Relocate SMM BASE during S3 resume
C8	S3_BEFORE_MP_INIT	Multi-processor initialization during S3 resume
C9	S3_BEFORE_RESTORE_ACPI_CALLBACK	Start to restore system configuration in SMM
CA	S3_AFTER_RESTORE_ACPI_CALLBACK	Restore system configuration in SMM complete
CB	S3_GO_TO_FACS_WAKING_VECTOR	Back to OS

ACPI

Table 30: ACPI 8-Bit POST Code Values

Value	Functionality Name	Description
51	ASL_ENTER_S1	Prepare to enter S1
53	ASL_ENTER_S3	Prepare to enter S3
54	ASL_ENTER_S4	Prepare to enter S4
55	ASL_ENTER_S5	Prepare to enter S5
E1	ASL_WAKEUP_S1	System wakeup from S1
E3	ASL_WAKEUP_S3	System wakeup from S3
E4	ASL_WAKEUP_S4	System wakeup from S4
E5	ASL_WAKEUP_S5	System wakeup from S5

SMM

Table 31: SMM 8-Bit POST Code Values

Value	Functionality Name	Description
A0	SMM_IDENTIFY_FLASH_DEVICE	Identify flash device in SMM
A2	SMM_SMM_PLATFORM_INIT	SMM service initialization
A6	SMM_ACPI_ENABLE_START	OS call ACPI enable function
A7	SMM_ACPI_ENABLE_END	ACPI enable function complete
A1	SMM_S1_SLEEP_CALLBACK	Enter S1
A3	SMM_S3_SLEEP_CALLBACK	Enter S3
A4	SMM_S4_SLEEP_CALLBACK	Enter S4
A5	SMM_S5_SLEEP_CALLBACK	Enter S5
A8	SMM_ACPI_DISABLE_START	OS call ACPI disable function
A9	SMM_ACPI_DISABLE_END	ACPI disable function complete

InsydeH2O DDT Debugger

Table 32: InsydeH2O DDT Debugger 8-Bit POST Code Values

Value	Functionality Name	Description
0D	Used by Insyde debugger	Waiting for device connect
D0	Used by Insyde debugger	Waiting for device connect
D1	Used by Insyde debugger	InsydeH2ODDT ready
D2	Used by Insyde debugger	EHCI not found
D3	Used by Insyde debugger	Debug port connect low speed device
D4	Used by Insyde debugger	DDT cable became low speed device
D5	Used by Insyde debugger	DDT cable transmission error (Get descriptor fail)
D6	Used by Insyde debugger	DDT cable transmission error (Set debug mode fail)
D7	Used by Insyde debugger	DDT cable transmission error (Set address fail)

Appendix D. Architectural Diagnostic Codes

Architectural Diagnostic diagnostic codes describe important events in the BIOS initialization sequence.

Table 33: Architectural Diagnostic Codes

Code	Symbol	Description
F0	SEC_ENTRY	SEC phase entry (reset vector)
F1	SEC_EXIT	SEC phase exit
F2	PEI_ENTRY	PEI phase entry (PEI dispatch)
F3	PEI_EXIT	PEI phase exit
F4	IPL_DXE	DXE IPL normal boot path
F5	IPL_S3	DXE IPL S3 boot path to OS
F6	S3_OS	S3 boot to OS
F7	IPL_RECOVERY	DXE IPL crisis recovery boot path
F8	IPL_EXIT	Exiting DXE IPL, starting DXE phase
F9	DXE_ENTRY	DXE dispatch start
FA	DXE_EXIT	DXE dispatch exit
FB	PEI_MEMORY	No permanent memory found in PEI phase
FC	PEI_IPL	No DXE IPL found in PEI phase
FD	IPL_DXE	No DXE found in IPL
FE	IPL_PPI	Missing PPIs needed by DXE
FF	DXE_ARCH	Missing architectural protocols at the end of DXE

Appendix E. Progress and Error Codes

Progress and error codes are only displayed on POST diagnostic displays that show four digits. On these displays, the most significant two digits show the progress or error code from the table in this section (Progress and Error Codes), while the least significant two digits show the diagnostic code (see tables above). For example: 0345 indicates the component was loaded, the DXE/UEFI entry point called, and DXE driver initialization of the HDD password feature.

Table 34: Progress and Error Codes

Code	Symbol	Description
01	COMP_PEI_BEGIN	The component was loaded and the PEI entry point called
02	COMP_PEI_END	The component returned from the entry point
03	COMP_DXE_BEGIN	The component was loaded and the DXE/UEFI entry point called
04	COMP_DXE_END	The component returned from the entry point
05	COMP_SUPPORTED	The Supported() member function of the component's instance of the Driver Binding protocol was called
06	COMP_START	The Start() member function of the component's instance of the Driver Binding protocol was called
07	COMP_STOP	The Stop() member function of the component's instance of the Driver Binding protocol was called
08	COMP_SMM_INIT	The component was loaded and the entry point called inside of SMM
09	DEVICE_ERROR	The driver encountered a condition where it cannot proceed due to a hardware failure
0A	RESOURCE_ERROR	The driver encountered a condition where it cannot proceed due to being unable to acquire resources
0B	DATA_CORRUPT	The driver encountered a condition where it found invalid data and could not continue
0C	COMP_PEI_CALLBACK	The component received a callback in PEI phase
0D	COMP_DXE_CALLBACK	The component received a callback in DXE phase

Appendix F. Warranty Information

Full warranty information can be found at https://winsystems.com/company-policies/warranty/.